BG77 Hardware Design

LPWA Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2020-01-10	Jake JIANG/ Rim HUANG/ Hyman DING	Initial
1.1	2021-01-08	Jake JIANG/ Rim HUANG/ Matt YE	1. Removed B14 for LTE Cat M1 and B26 for LTE Cat NB2. 2. Updated GNSS function into a standard configuration. 3. Updated the dimensional tolerance of the module in Table 2 and Chapter 7. 4. Enabled fast shutdown interface (realized through pin 63 GPIO7) and added the description thereof in Chapter 3.6.3. 5. Updated the reference design of PON_TRIG in Figure 13. 6. Updated the GNSS performance in Table 27. 7. Updated the current consumption values in Table 36. 8. Added the GNSS current consumption values in Table 37. 9. Updated the RF receiving sensitivity in Table 39. 10. Updated the electrostatic discharge characteristics in Table 40. 11. Updated the storage conditions in Chapter 8.1. 12. Updated the recommended stencil thickness and the recommended reflow soldering thermal profile parameters in Chapter 8.2.
1.2	2021-09-16	Lex LI	1. Added the high-speed operation mode of USB interface in Chapter 2.2 and 3.10. 2. Updated the USB serial driver information in Chapter 2.2. 3. Updated the way of waking up the module from PSM

	with the PON_TRIG pin in Chapter 3.8. 4. Completed the GNSS performance data in Table 28. 5. Updated unspecified dimensional tolerances from ±0.05 mm to ±0.2 mm in Chapter 7. 6. Updated recommended reflow soldering thermal profile parameters and added some notes about manufacturing and soldering in Chapter 8.2. 7. Optimized packaging specifications in Chapter 8.3.

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1 Introduction

This document defines BG77 module and describes its air interface and hardware interfaces which connect to your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of BG77. To facilitate application designs, it also includes some reference designs. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

2.1. General Description

BG77 is an embedded IoT (LTE Cat M1, LTE Cat NB2) wireless communication module. It provides data connectivity on LTE-FDD network, and supports half-duplex operation in LTE network. It also provides GNSS and voice [1] functionality to meet your specific application demands.

The module is based on an architecture in which WWAN (LTE) and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. For more details, see ***document [1]***.

BG77 is an industrial-grade module for industrial and commercial applications only.

Table 2: Frequency Bands and GNSS Types of BG77 Module

Supported Bands	Power Class	GNSS
Cat M1: LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/ B26/B27/B28/B66/B85* **Cat NB2 [2]:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/ B28/B66/B71/B85*	Power Class 5 (21 dBm)	GPS, GLONASS, BeiDou, Galileo, QZSS

With a compact profile of 14.9 mm × 12.9 mm × 1.7 mm, BG77 can meet almost all requirements for M2M applications such as smart metering, tracking system, security, wireless POS, etc. It is especially suitable for size and weight sensitive applications such as smart watch and other wearable devices.

[1] BG77 supports VoLTE (Voice over LTE) under LTE Cat M1 only.
[2] LTE Cat NB2 is backward compatible with LTE Cat NB1.

BG77 is an SMD type module which can be embedded into applications through its 94 LGA pins. It supports internet service protocols like TCP, UDP and PPP. Based on extended AT commands developed by Quectel, you can use these internet service protocols easily.

2.2. Key Features

Table 3: Key Features of BG77

Features	Details
Power Supply [3]	● Supply voltage: 2.6–4.8 V ● Typical supply voltage: 3.3 V
Transmitting Power	Class 5 (21 dBm +1.7/-3 dB) for LTE-FDD bands
LTE Features	● Support 3GPP Rel-14 ● Support LTE Cat M1 and LTE Cat NB2 ● Support 1.4 MHz RF bandwidth for LTE Cat M1 ● Support 200 kHz RF bandwidth for LTE Cat NB2 ● Cat M1: Max. 588 kbps (DL)/Max. 1119 kbps (UL) ● Cat NB2: Max. 127 kbps (DL)/ Max. 158.5 kbps (UL)
Internet Protocol Features	● Support PPP/TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/NITZ/PING/MQTT/ LwM2M/CoAP/IPv6 protocols ● Support PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V USIM/SIM card only
PCM Interface	Supports one digital audio interface: PCM interface for VoLTE only
USB Interface	● Compliant with USB 2.0 specification (slave only) ● Support operations at high-speed, full-speed and low-speed ● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade ● Support USB serial drivers for Windows 7/8/8.1/10, Linux 2.6–5.12, Android 4.x–11.x
UART Interfaces	**Main UART:** ● Used for data transmission and AT command communication

[3] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

	● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for software debugging and log output ● Support 115200 bps baud rate **GNSS UART:** ● Used for GNSS NMEA sentences output ● 115200 bps baud rate by default
GNSS	● GPS, GLONASS, BeiDou, Galileo and QZSS ● 1 Hz data update rate by default
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Network Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Dimensions: (14.9 ±0.2) mm × (12.9 ±0.2) mm × (1.7 ±0.2) mm ● Weight: approx. 0.73 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [4] ● Extended temperature range: -40 °C to +85 °C [5] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of BG77 and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

[4] Within the operating temperature range, the module meets 3GPP specifications.
[5] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

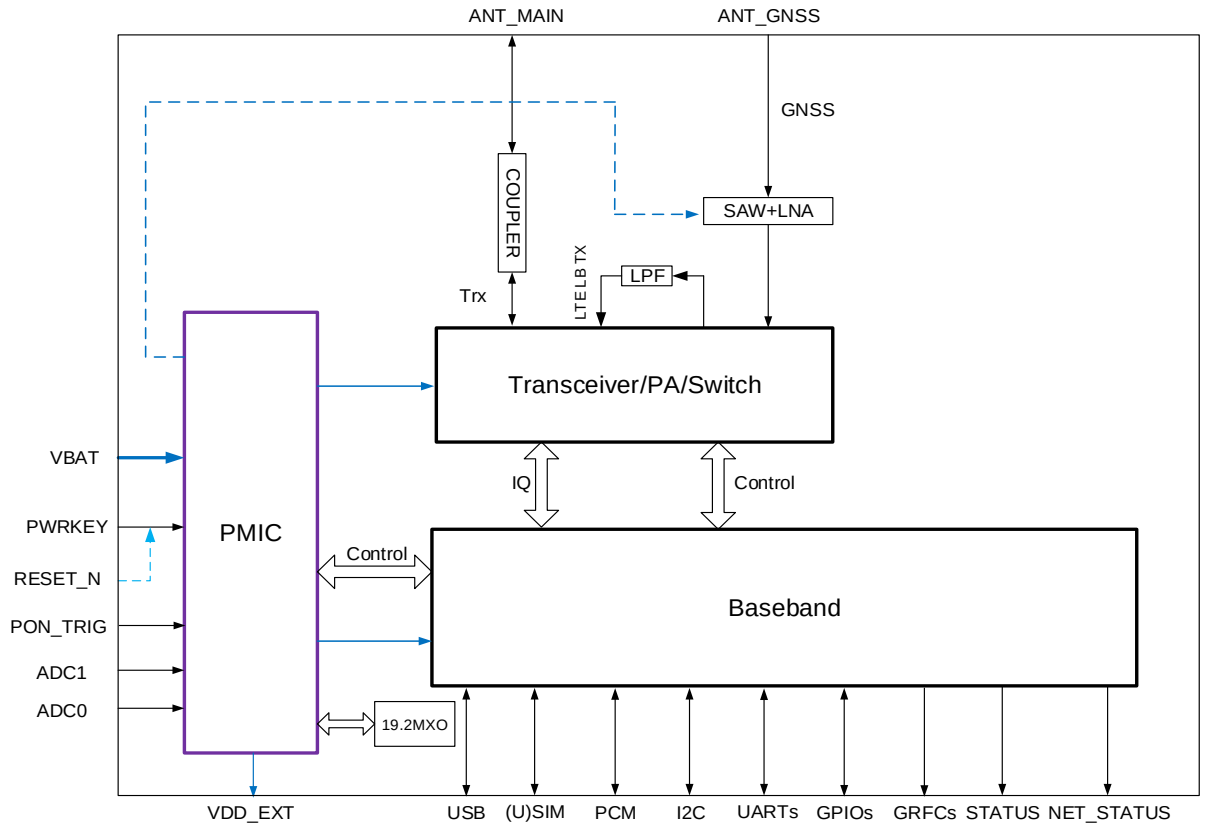


Figure 1: Functional Diagram

NOTE

1. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
2. RESET_N connects directly to PWRKEY inside the module.

2.4. EVB

To facilitate application development with BG77 conveniently, Quectel supplies the evaluation board (EVB), USB to RS-232 converter cable, USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [2]***.

3 Application Interfaces

BG77 is equipped with 94 LGA pins for connection to various cellular application platforms. The subsequent chapters provide detailed description of interfaces listed below:

- Power supply
- PON_TRIG Interface
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- Network status indication
- STATUS
- MAIN_RI
- USB_BOOT interface
- ADC interfaces
- GPIO interfaces
- GRFC interfaces

3.1. Pin Assignment

The following figure shows the pin assignment of BG77.

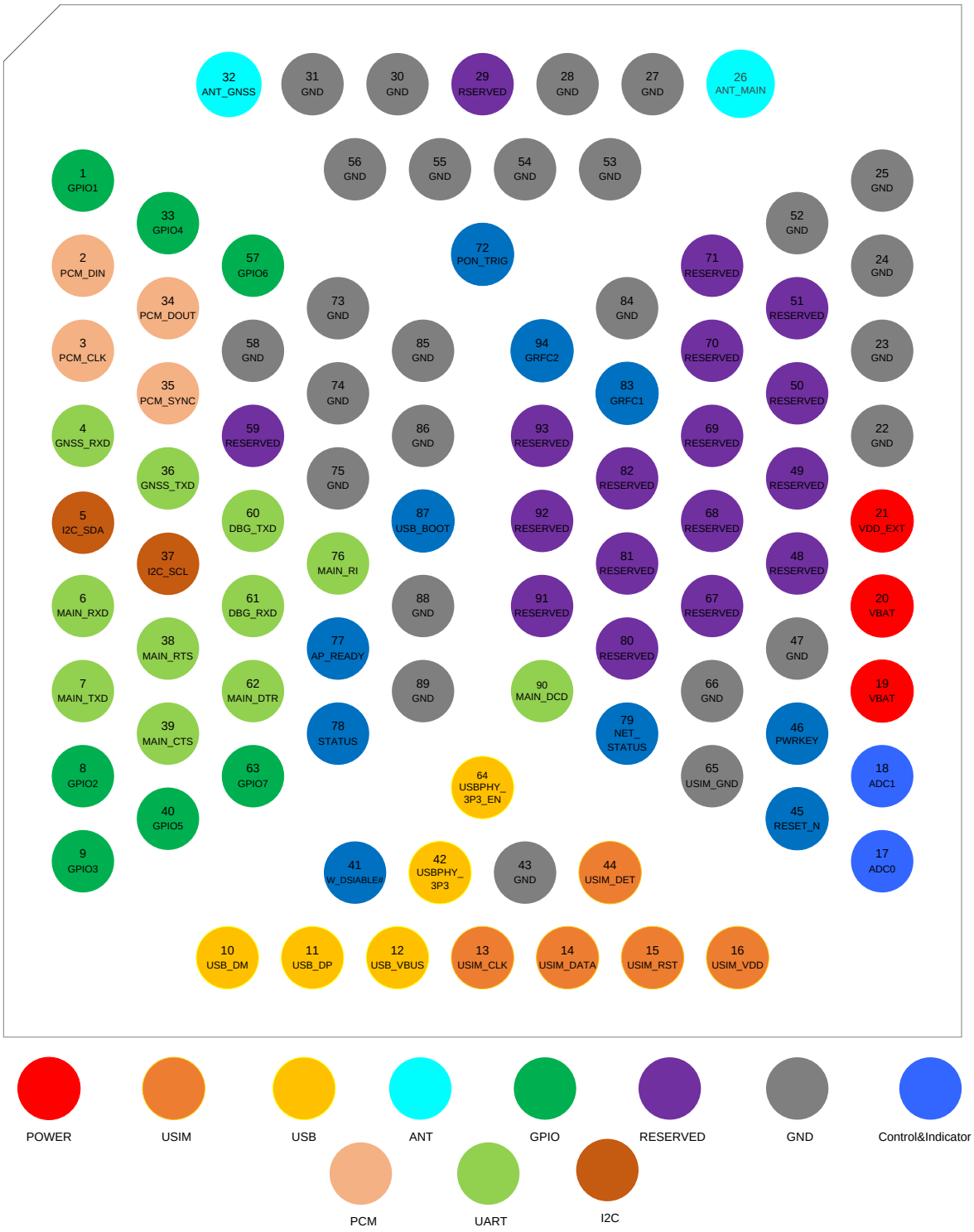


Figure 2: Pin Assignment (Top View)

NOTE

1. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
2. RESET_N connects directly to PWRKEY inside the module.
3. ADC input voltage must not exceed 1.8 V.
4. The input voltage range of USB_VBUS is 1.3–1.8 V.
5. GPIO5 (pin 40), NET_STATUS (pin 79) and GRFC1 (pin 83) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
6. GPIO7 (pin 63) supports fast shutdown function. The function is disabled by default. See ***Chapter 3.6.3*** for more details.
7. PCM and I2C interfaces are for VoLTE only.
8. Keep all RESERVED pins and unused pins unconnected.
9. Connect GND pins to ground in the design.

3.2. Pin Description

The following tables show the pin definition and description of BG77.

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	19, 20	PI	Power supply for the module	Vmax = 4.8 V Vmin = 2.6 V Vnom = 3.3 V	See NOTE 1.
VDD_EXT	21	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	If unused, keep this pin open.
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	46	DI	Turn on/off the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Never pull down PWRKEY to GND permanently.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	45	DI	Reset the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connects directly to PWRKEY inside the module).
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	78	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep this pin open.
NET_STATUS	79	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_VBUS	12	AI	USB connection detect	V_{IH}max = 1.8 V V_{IH}min = 1.3 V	
USB_DP	11	AIO	USB differential data (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Vnom = 3.3 V	
USBPHY_3P3_EN	64	DO	External LDO enable control for USB	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	44	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	16	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	15	DO	(U)SIM card reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_DATA	14	DIO	(U)SIM card data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_CLK	13	DO	(U)SIM card clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_GND	65		Specified ground for (U)SIM card		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	62	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RXD	6	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep this pin

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	open.
MAIN_TXD	7	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_CTS	39	DO	DTE clear to send signal from DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RTS	38	DI	DTE request to send signal from DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_DCD	90	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RI	76	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	61	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
DBG_TXD	60	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
GNSS UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_TXD	36	DO	GNSS UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
GNSS_RXD	4	DI	GNSS UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PCM_CLK	3	DO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_SYNC	35	DO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_DIN	2	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM_DOUT	34	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	37	OD	I2C serial clock (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep this pin open.
I2C_SDA	5	OD	I2C serial data (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep this pin open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	26	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	32	AI	GNSS antenna interface		50 Ω impedance. If unused, keep this pin open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	1	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep this pin open.

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
GPIO2	8	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO3	9	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO4	33	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO5	40	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GPIO6	57	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO7	63	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. GPIO by default, and can be multiplexed into fast shutdown interface (see ***Chapter 3.6.3*** for details). If unused, keep this pin open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC0	17	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep this pin open.
ADC1	18	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep this pin open.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	41	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When it is at low level, the module can enter airplane mode. If unused, keep this pin open.
AP_READY	77	DI	Application processor sleep state detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USB_BOOT	87	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PON_TRIG	72	DI	Wake up the module from PSM		1.8 V power domain. Rising-edge triggered. Pulled-down by default. If unused, keep this pin open.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GRFC2	94	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	29, 48–51, 59, 67–71, 80–82, 91–93	Keep these pins open.

NOTE

1. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
3. RESET_N connects directly to PWRKEY inside the module.
4. The input voltage range of USB_VBUS is 1.3–1.8 V.
5. USBPHY_3P3 and USBPHY_3P3_EN pins are used for USB PHY circuits.
6. GPIO5 (pin 40), NET_STATUS (pin 79) and GRFC1 (pin 83) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
7. GPIO7 (pin 63) supports fast shutdown function. The function is disabled by default. See ***Chapter 3.6.3*** for more details.
8. ADC input voltage must not exceed 1.8 V.
9. PCM and I2C interfaces are for VoLTE only.
10. Keep all RESERVED pins and unused pins unconnected.

3.3. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Connected	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module into airplane mode where the	

	RF function is invalid.
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.
Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption is reduced to a low level.
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT) remains applied.
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The power consumption is reduced to a minimized level.

NOTE

During e-I-DRX, it is recommended to use UART interface for data communication, as the use of USB interface increases power consumption.

3.4. Power Saving

3.4.1. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible. This mode can be set via the following ways.

Hardware:

W_DISABLE# is pulled up by default. Driving it low makes the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**. For details of the command, see ***document [6]***.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.4.2. Power Saving Mode (PSM)

The module minimizes its power consumption through entering PSM. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, the module in PSM cannot immediately respond to users' requests.

When the module wants to use the PSM, it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g. when the conditions are changed in the module, the module requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS**.

Any of the following methods can wake up the module from PSM:

- Wake up the module from PSM through a rising edge on PON_TRIG. (recommended)
- Wake up the module by driving PWRKEY low.
- When the T3412_Ext timer expires, the module wakes up from PSM automatically.

NOTE

See ***document [3]*** for details about **AT+CPSMS**.

3.4.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length

value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what were requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by **AT+CEDRXS=1**.

NOTE

See ***document [3]*** for details about **AT+CEDRXS**.

3.4.4. Sleep Mode

The module is able to reduce its power consumption to a lower value during the sleep mode. The following sub-chapters describe the power saving procedure of the module.

3.4.4.1. UART Application Scenario

If the host communicates with the module via UART interface, the following preconditions enable the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

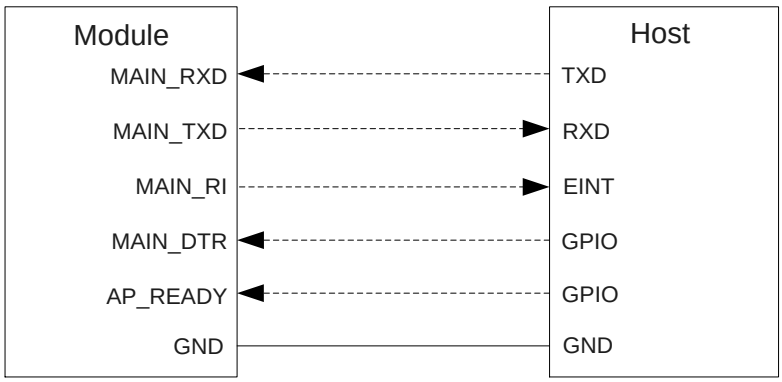


Figure 3: Sleep Mode Application via UART

- When the module has a URC to report, MAIN_RI will wake up the host. See ***Chapter 3.15*** for details about MAIN_RI behavior.
- Driving MAIN_DTR low will wake up the module.
- AP_READY detects the sleep state of the host (can be configured to high voltage level or low voltage level detection). See **AT+QCFG="apready"** in ***document [6]*** for details.

3.5. Power Supply

3.5.1. Power Supply Pins

BG77 provides two VBAT pins for connection with an external power supply.

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT [6]	19, 20	Power supply for the module	2.6	3.3	4.8	V
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89					

3.5.2. Voltage Stability Requirements

The power supply range of BG77 is from 2.6 V to 4.8 V. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V. Make sure that the input voltage never drops below 2.6 V.

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The width of VBAT trace should be no less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to get a stable power source, it is suggested to use a TVS with low leakage current and suitable reverse stand-off voltage, and also it is recommended to place it as close to the VBAT pins as possible. The following figure shows a reference circuit of the power supply.

[6] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

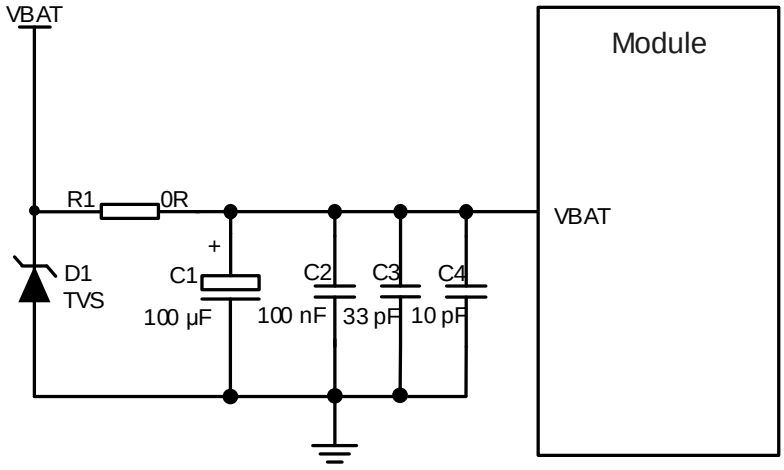


Figure 4: Reference Circuit of the Power Supply

Power design for a module is critical to its performance. The power supply of BG77 should be able to provide sufficient current of 0.7 A at least, and it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output no less than 1.0 A for the power supply design.

3.5.3. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT voltage value. For more details, see ***document [3]***.

3.6. Turn on and off Scenarios

3.6.1. Turn on with PWRKEY

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	46	Turn on/off the module	Vnom = 1.5 V V_{IL}max = 0.45 V	The output voltage is 1.5 V because of the voltage drop inside the chipset.

When the module is in power off mode, it can be turned on by driving PWRKEY low for 500–1000 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

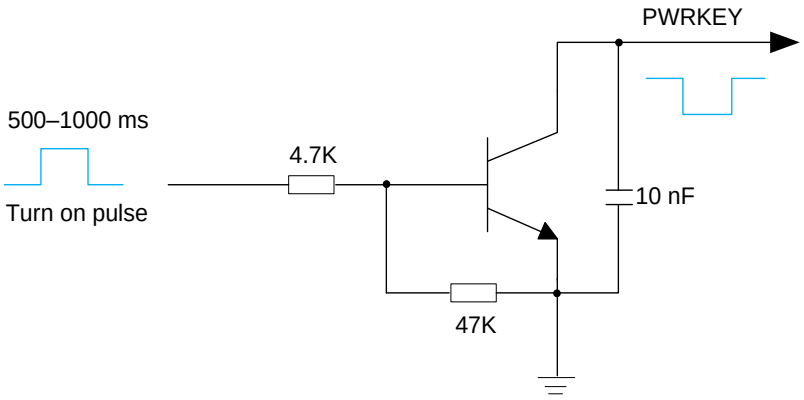


Figure 5: Turn on the Module with a Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

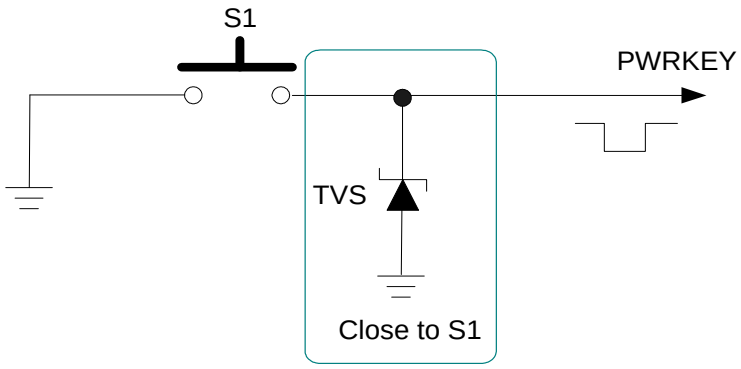


Figure 6: Turn on the Module with a Button

The power-up scenario is illustrated in the following figure.

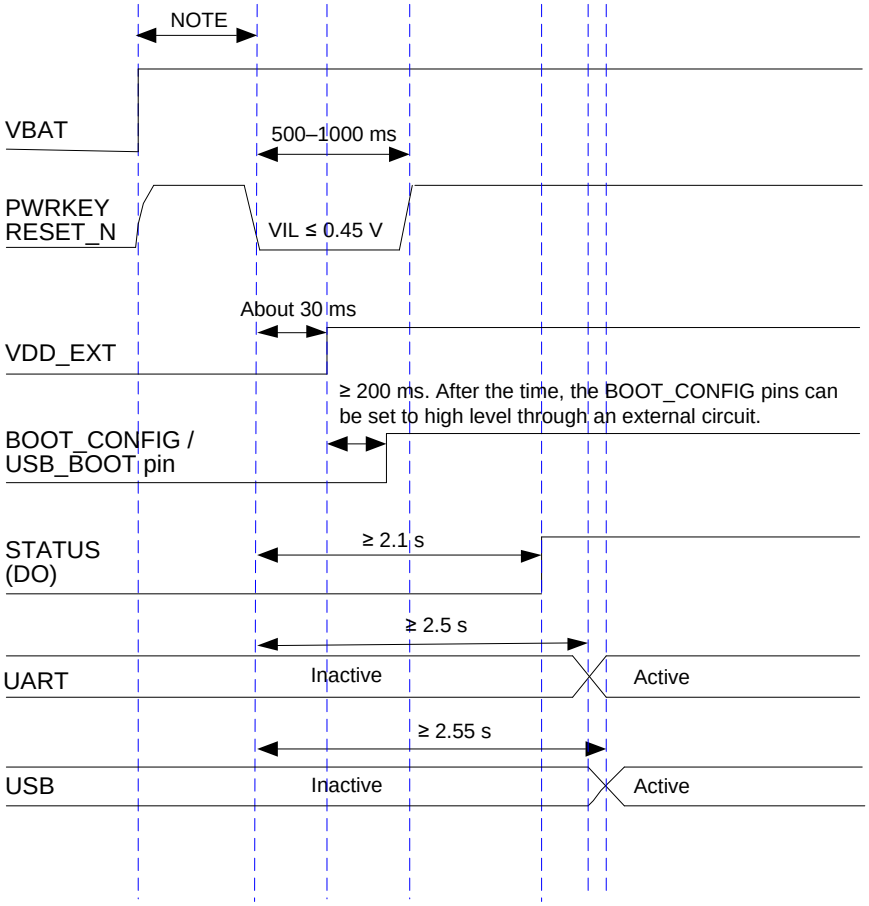


Figure 7: Power-up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY and keep the interval no less than 30 ms.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

3.6.2. Turn off

Either of the following methods can be used to turn off the module:

- Turn off the module with PWRKEY.
- Turn off the module with **AT+QPOWD**.

3.6.2.1. Turn off with PWRKEY

Driving PWRKEY low for 650–1500 ms and then releasing it, the module will execute power-down procedure.

The power-down scenario is illustrated in the following figure.

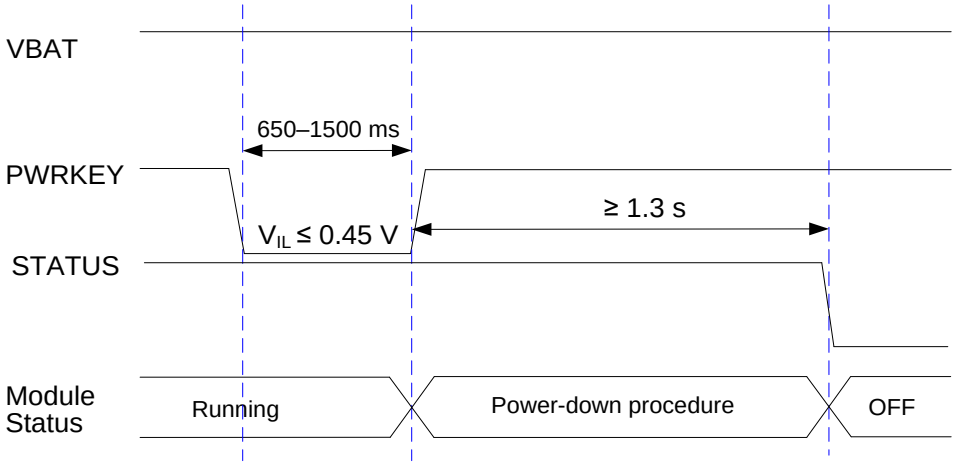


Figure 8: Power-down Timing

3.6.2.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module with PWRKEY.

See ***document [3]*** for details about **AT+QPOWD**.

3.6.3. Fast Shutdown

The module supports fast shutdown function through GPIO7 (pin 63). When the pin detects a falling edge, the module powers off within 100 ms without damaging the filesystem, but the writing data may be lost.

Fast shutdown is disabled by default. For details, see **AT+QCFG="fast/poweroff"** in ***document [6]***.

Table 9: Pin Definition of Fast Shutdown Interface

Pin Name	Pin No.	I/O	Description	Comment
GPIO7 [7]	63	DI	When the pin detects a falling edge, the module powers off within 100 ms.	Falling-edge triggered. Pulled-up by default. 1.8 V power domain.

The fast shutdown timing is illustrated in the following figure.

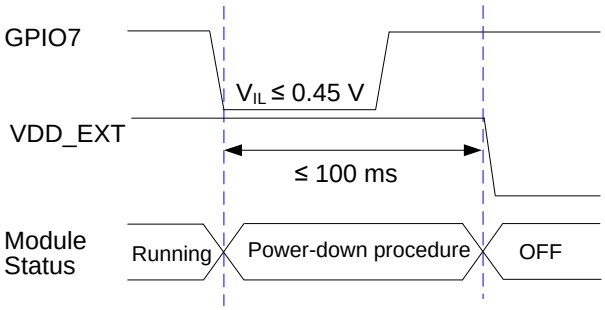


Figure 9: Fast Shutdown Timing

3.7. Reset

RESET_N is used to reset the module. Due to platform limitations, the chipset has integrated the reset function into PWRKEY, and RESET_N connects directly to PWRKEY inside the module.

The module can be reset by driving RESET_N low for 2–3.8 s.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	45	Reset the module	V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connects directly to PWRKEY inside the module).

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

[7] Pin 63 is a general-purpose GPIO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG ="fast/poweroff"**.

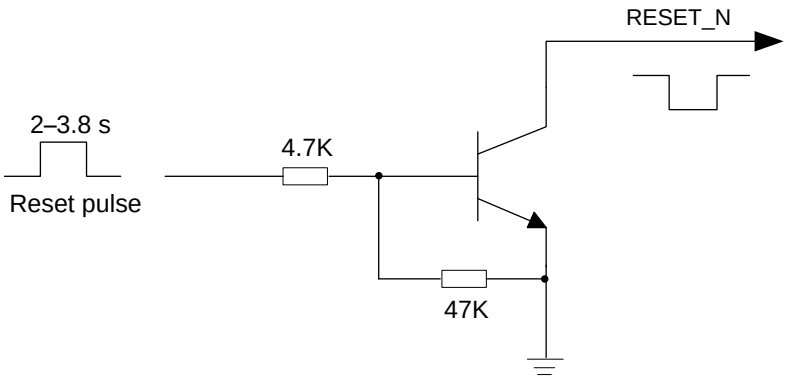


Figure 10: Reference Circuit of RESET_N with a Driving Circuit

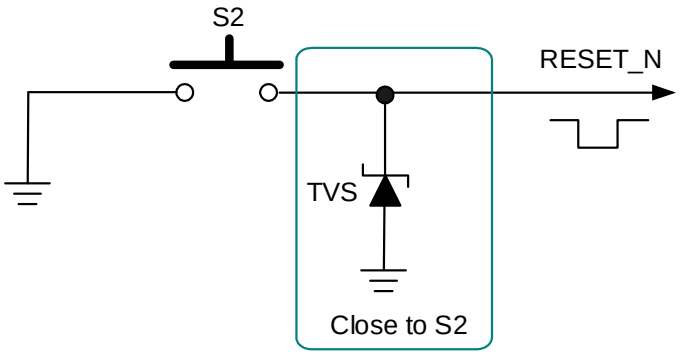


Figure 11: Reference Circuit of RESET_N with a Button

The reset timing is illustrated in the following figure.

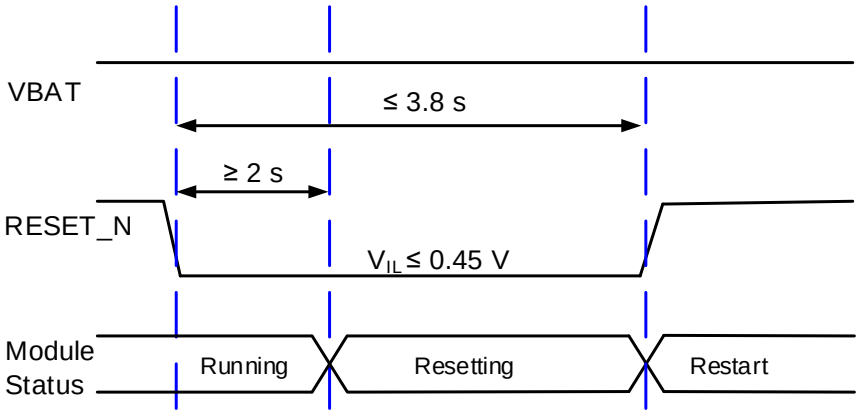


Figure 12: Reset Timing

NOTE

Ensure that there is no large capacitance on RESET_N pin.

3.8. PON_TRIG Interface

BG77 provides one PON_TRIG pin which is used to wake up the module from PSM. When the pin detects a rising edge and keeps at high level for at least 30 ms, the module will wake up from PSM.

Table 11: Pin Definition of PON_TRIG Interface

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	72	DI	Wake up the module from PSM	Rising-edge triggered. Pulled-down by default. 1.8 V power domain.

A reference circuit is shown in the following figure.

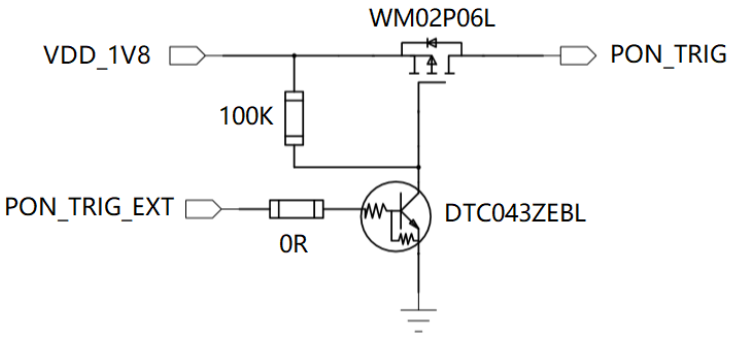


Figure 13: Reference Circuit of PON_TRIG

NOTE

VDD_1V8 is provided by an external LDO.

3.9. (U)SIM Interface

BG77 supports 1.8 V (U)SIM card only. The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements.

Table 12: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	44	DI	(U)SIM card hot-plug detect	1.8 V power domain.
USIM_VDD	16	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.
USIM_RST	15	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	14	DIO	(U)SIM card data	1.8 V power domain.
USIM_CLK	13	DO	(U)SIM card clock	1.8 V power domain.
USIM_GND	65		Specified ground for (U)SIM card	

BG77 supports (U)SIM card hot-plug via USIM_DET, and both high and low level detections are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [3]*** for more details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

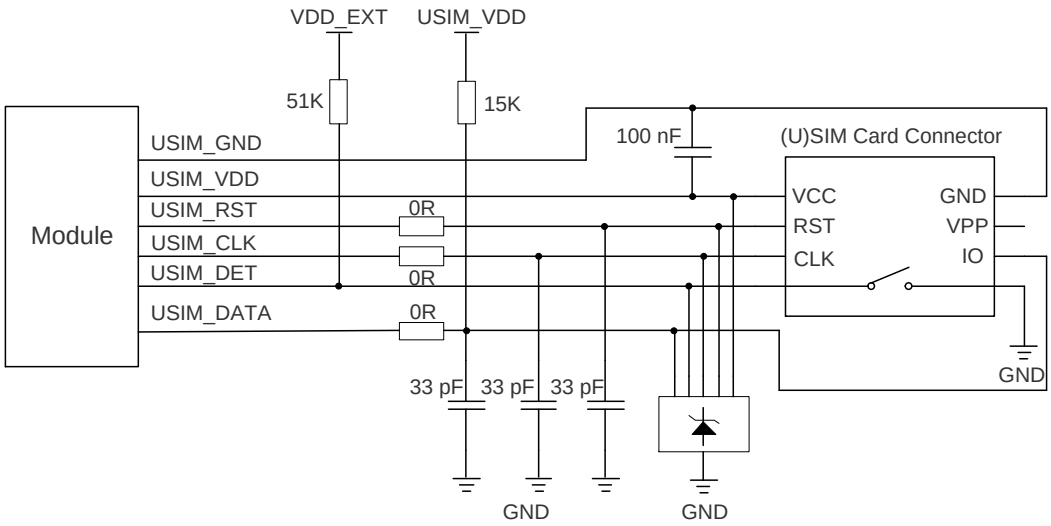


Figure 14: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

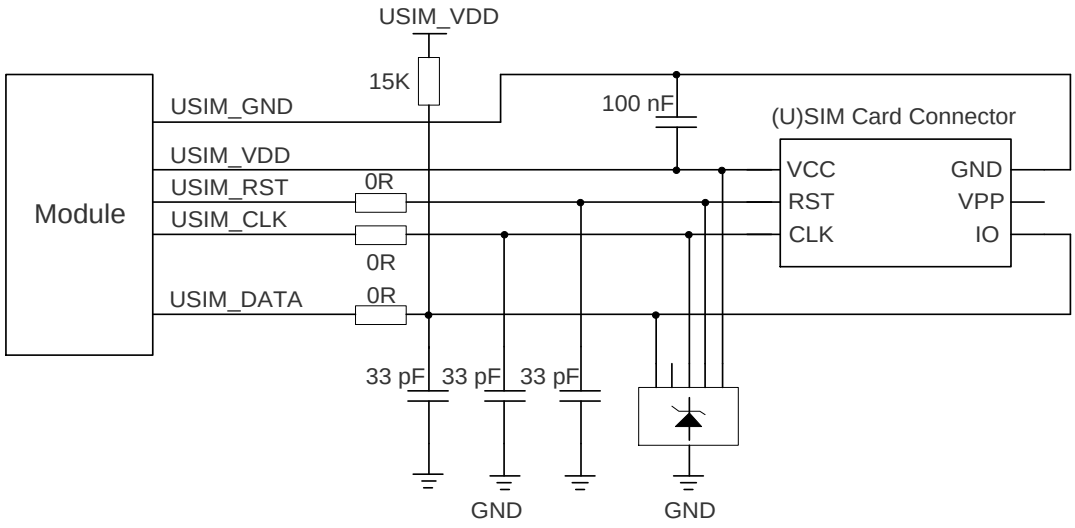


Figure 15: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be surrounded with ground.
- To offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. To facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

BG77 provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification. BG77 can only be used as a slave device and supports operation at low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps) modes .

The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DM	10	AIO	USB differential data (-)	Require differential impedance of 90 Ω.
USB_DP	11	AIO	USB differential data (+)	
USB_VBUS	12	AI	USB connection detect	Input voltage range: 1.3–1.8 V
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Vnom = 3.3 V
USBPHY_3P3_EN	64	DO	External LDO enable control for USB	1.8 V power domain
GND	43	-	Ground	

For more details about USB 2.0 specification, visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade and software debugging in application designs. The following figures illustrate reference designs of USB PHY and USB interface.

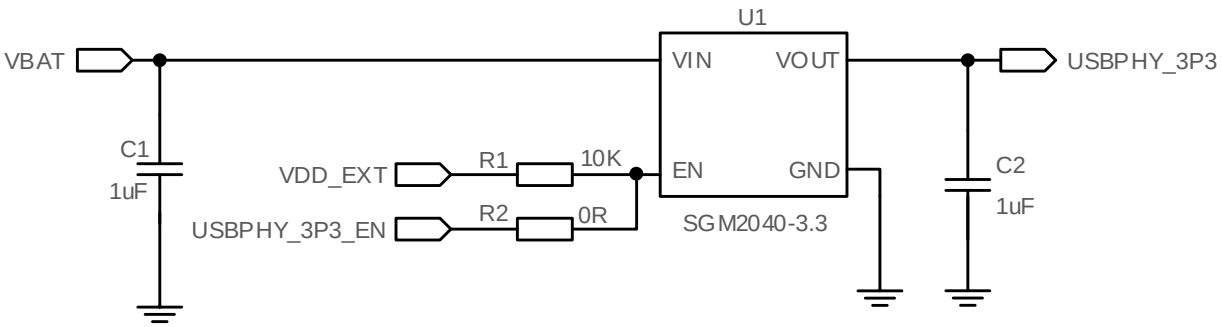


Figure 16: Reference Design of USB PHY

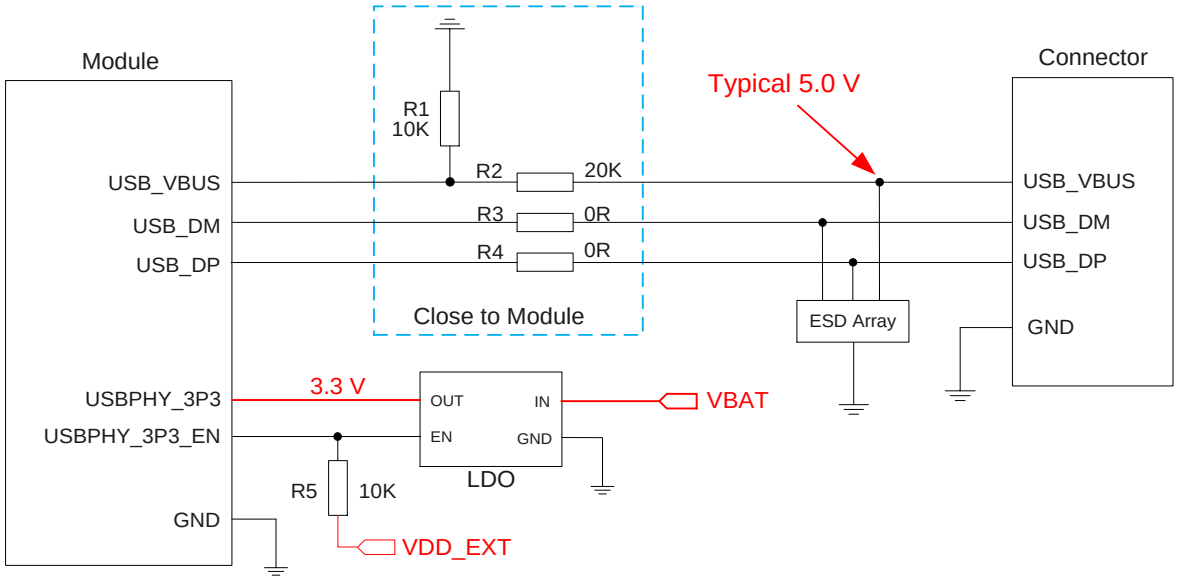


Figure 17: Reference Design of USB Interface

To ensure the integrity of USB data line signal, resistors R3 and R4 should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection devices as close to the USB connector as possible.

NOTE

The input voltage range of USB_VBUS is 1.3–1.8 V.

3.11. UART Interfaces

The module provides three UART interfaces: the main UART, debug UART and the GNSS UART interfaces. Features of them are illustrated below:

- The main UART interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bps baud rates, and the default baud rate is 115200 bps. It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART interface supports a fixed baud rate of 115200 bps, and is used for software debugging and log output.
- The GNSS UART interface supports 115200 bps baud rate by default, and is used for GNSS NMEA sentences output.

Table 14: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	1.8 V power domain
MAIN_RXD	6	DI	Main UART receive	1.8 V power domain
MAIN_TXD	7	DO	Main UART transmit	1.8 V power domain
MAIN_CTS	39	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	1.8 V power domain
MAIN_RTS	38	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	1.8 V power domain
MAIN_DCD	90	DO	Main UART data carrier detect	1.8 V power domain
MAIN_RI	76	DO	Main UART ring indication	1.8 V power domain

NOTE

AT+IPR can be used to set the baud rate of the main UART interface, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). See ***document [3]*** for more details about these AT commands.

Table 15: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	60	DO	Debug UART transmit	1.8 V power domain
DBG_RXD	61	DI	Debug UART receive	1.8 V power domain

Table 16: Pin Definition of GNSS UART Interface

Pin Name	Pin No.	I/O	Description	Comment
GNSS_TXD	36	DO	GNSS UART transmit	1.8 V power domain
GNSS_RXD	4	DI	GNSS UART receive	1.8 V power domain

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. The voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design of the main UART interface:

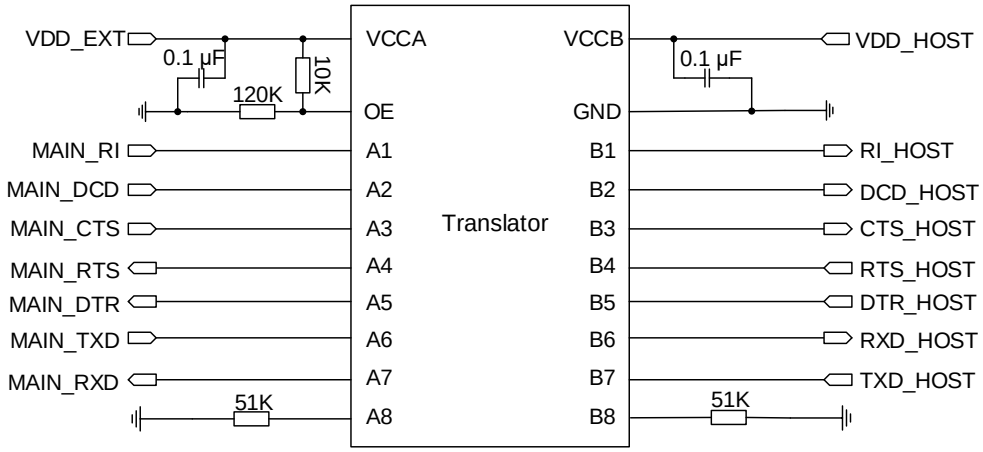


Figure 18: Main UART Reference Design (Translator Chip)

Visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

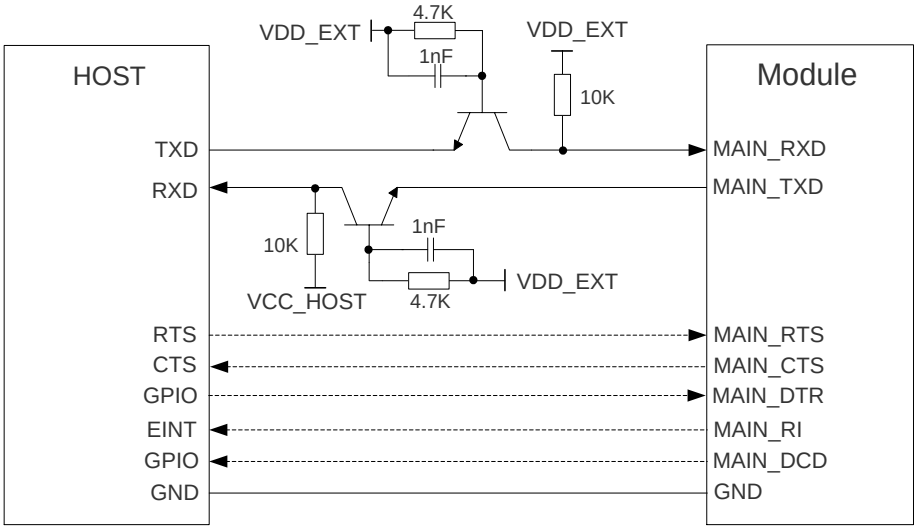


Figure 19: Main UART Reference Design (Transistor Circuit)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.12. PCM and I2C Interfaces

BG77 provides one Pulse Code Modulation (PCM) digital interface and one I2C interface for VoLTE only. The following table shows the pin definition of the two interfaces which can be applied on audio codec design.

Table 17: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	2	DI	PCM data input	1.8 V power domain
PCM_CLK	3	DO	PCM clock	1.8 V power domain
PCM_DOUT	34	DO	PCM data output	1.8 V power domain
PCM_SYNC	35	DO	PCM data frame sync	1.8 V power domain

I2C_SDA	5	OD	I2C serial data (for external codec)	Require external pull-up to 1.8 V
I2C_SCL	37	OD	I2C serial clock (for external codec)	Require external pull-up to 1.8 V

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

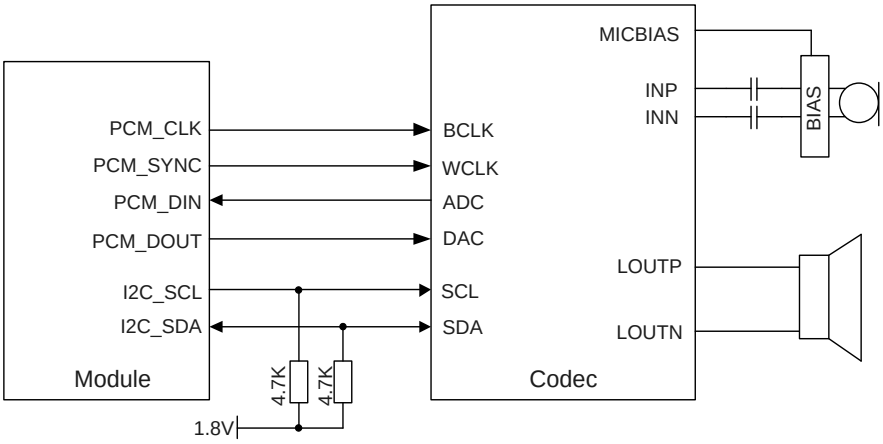


Figure 20: Reference Circuit of PCM Application with Audio Codec

NOTE

PCM and I2C interfaces support VoLTE only.

3.13. Network Status Indication

BG77 provides one network status indication pin: NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 18: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	79	DO	Indicate the module's network activity status	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.

Table 19: Working State of NET_STATUS

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

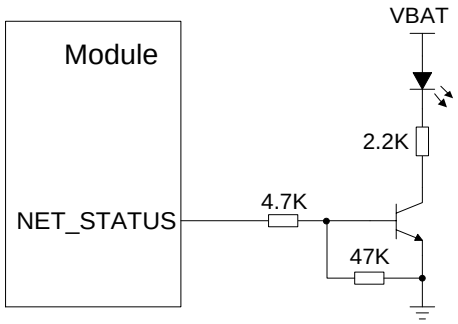


Figure 21: Reference Design of NET_STATUS

NOTE

NET_STATUS is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power on normally.

3.14. STATUS

The STATUS pin indicates the operation status of BG77. It outputs high level when the module powers on.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	78	DO	Indicate the module's operation status	1.8 V power domain

The following figure shows a reference circuit of STATUS.

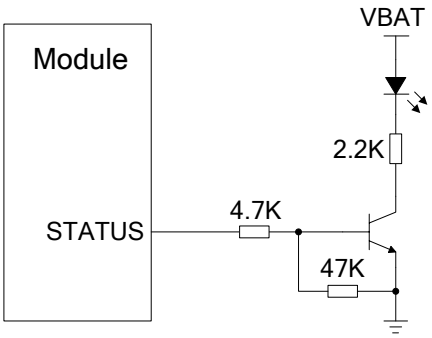


Figure 22: Reference Design of STATUS

3.15. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, a URC will trigger the behavior of MAIN_RI pin.

The default behaviors of MAIN_RI are shown as below.

Table 21: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps in high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The default MAIN_RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"**. For more details about **AT+QCFG**, see ***document [6]***.

NOTE

A URC can be outputted from UART port and USB modem port, through configuration via **AT+QURCCFG** (see ***document [3]*** for details). The default port is USB modem port.

3.16. USB_BOOT Interface

BG77 provides a USB_BOOT pin. During development or factory production, USB_BOOT can force the module to boot from USB port for firmware upgrade.

Table 22: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	87	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

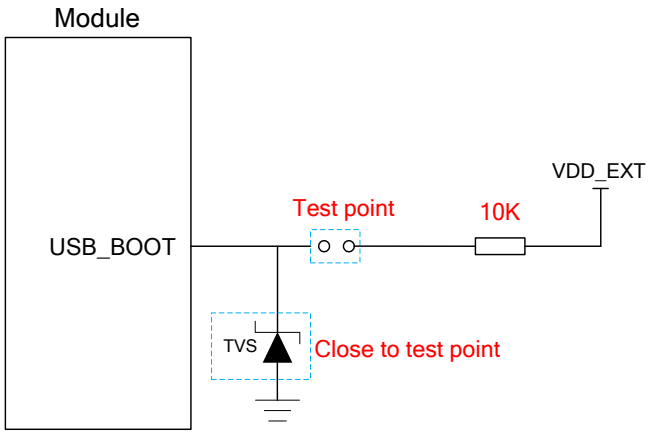


Figure 23: Reference Design of USB_BOOT Interface

The following figure shows the timing of USB_BOOT.

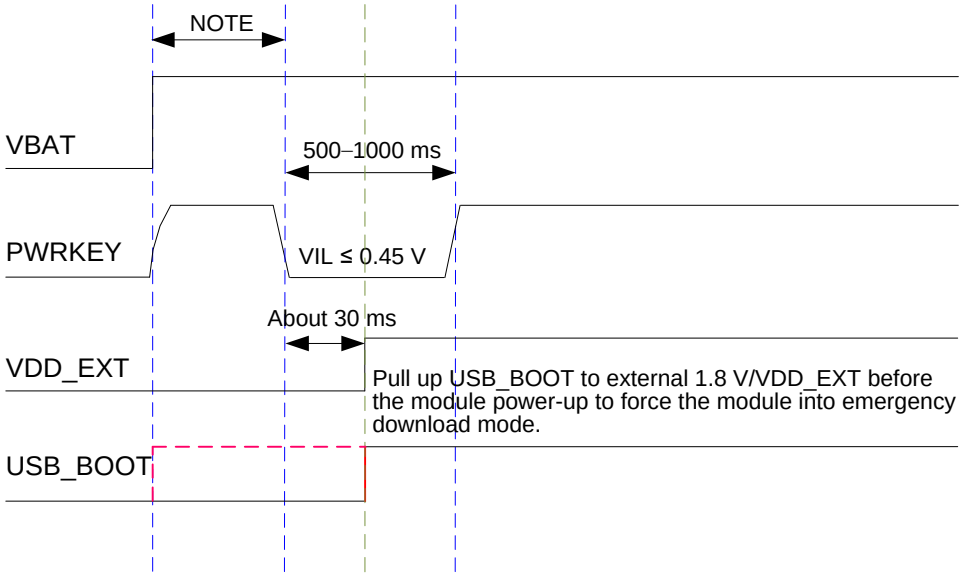


Figure 24: Timing of Turning on Module with USB_BOOT

NOTE

1. It is recommended to reserve the above circuit design during application design.
2. Ensure that VBAT is stable before pulling down PWRKEY. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY is no less than 30 ms.
3. When using MCU to control the module entering emergency download mode, follow the above timing sequence. Connecting the test points as shown in ***Figure 23*** can manually force the module to enter download mode.

3.17. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about the AT command, see ***document [3]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description
ADC0	17	AI	General-purpose ADC interface
ADC1	18	AI	General-purpose ADC interface

Table 24: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0.1	-	1.8	V
Resolution (LSB)	-	64.979	-	μV
Analog Bandwidth	-	500	-	kHz
Sample Clock	-	4.8	-	MHz
Input Resistance	10	-	-	MΩ

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider's resistor accuracy should be no less than 1 %.

3.18. GPIO Interfaces

BG77 module provides seven general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** can be used to configure the status of GPIO pins. For more details about the AT command, see ***document [6]***.

Table 25: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description
GPIO1	1	DIO	General-purpose input/output

GPIO2	8	DIO	General-purpose input/output
GPIO3	9	DIO	General-purpose input/output
GPIO4	33	DIO	General-purpose input/output
GPIO5 [8]	40	DIO	General-purpose input/output
GPIO6	57	DIO	General-purpose input/output
GPIO7 [9]	63	DIO	General-purpose input/output

3.19. GRFC Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 26: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comments
GRFC1 [10]	83	DO	Generic RF controller	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.
GRFC2	94	DO	Generic RF controller	1.8 V power domain.

Table 27: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	880–2200	B1, B2, B3, B4, B8, B25, B66
Low	High	791–894	B5, B18, B19, B20, B26, B27
High	Low	698–803	B12, B13, B28, B85*
High	High	617–698	B71

[8] GPIO5 (pin 40) is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power on normally.
[9] GPIO7 (pin 63) is a general-purpose GPIO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG="fast/poweroff"**. See ***Chapter 3.6.3*** for details.
[10] GRFC1 (pin 83) is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power on normally.

4 GNSS

4.1. General Description

BG77 includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BeiDou, Galileo and QZSS.

The module supports standard *NMEA-0183* protocol, and outputs GNSS NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, BG77 GNSS engine is switched off. It has to be switched on via AT command. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [1]***.

4.2. GNSS Performance

Table 28: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-145	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	31.22	s
		XTRA enabled	9.52	s
	Warm start @ open sky	Autonomous	30.74	s
		XTRA enabled	2.51	s
	Hot start @ open sky	Autonomous	1.43	s

		XTRA enabled	1.47	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	< 2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between GNSS antenna and main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

Refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG77 includes a main antenna interface and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

Table 29: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	26	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 30: BG77 Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B18	815–830	860–875	MHz

LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26 [11]	814–849	859–894	MHz
LTE-FDD B27 [11]	807–824	852–869	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz
LTE-FDD B71 [12]	663–698	617–652	MHz
LTE-FDD B85*	698–716	728–746	MHz

5.1.3. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

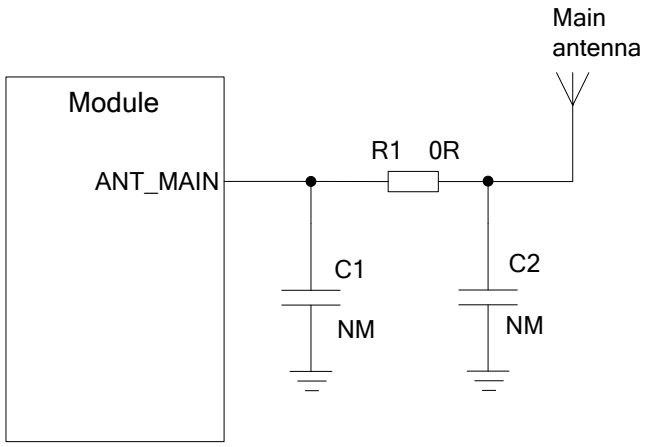


Figure 25: Reference Design of Main Antenna Interface

[11] LTE-FDD B26 and B27 are supported by LTE Cat M1 only.
[12] LTE-FDD B71 is supported by LTE Cat NB2 only.

5.2. GNSS Antenna Interface

5.2.1. Pin Definition

Table 31: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	32	AI	GNSS antenna interface	50 Ω impedance

5.2.2. GNSS Operating Frequency

Table 32: GNSS Operating Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou	1561.098 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

5.2.3. Reference Design

A reference design of GNSS antenna interface is shown as below.

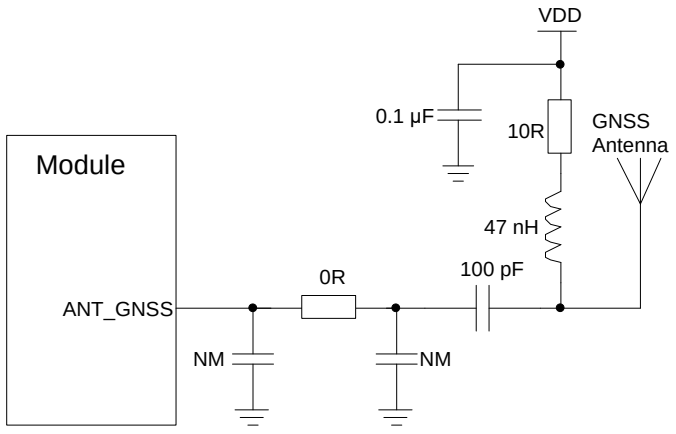


Figure 26: Reference Circuit of GNSS Antenna Interface

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. RF Routing Guidelines

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

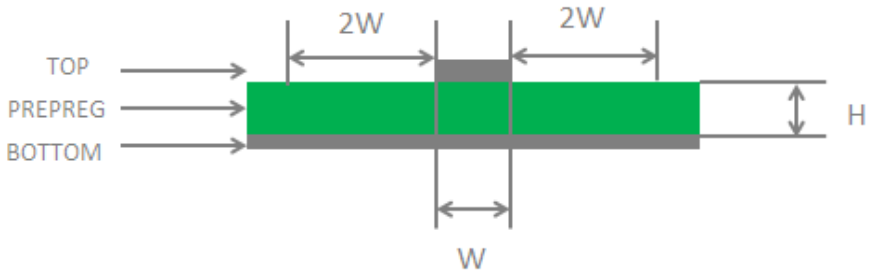


Figure 27: Microstrip Design on a 2-layer PCB

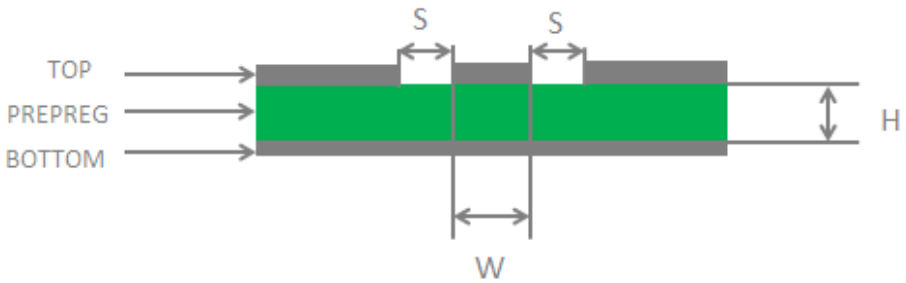


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

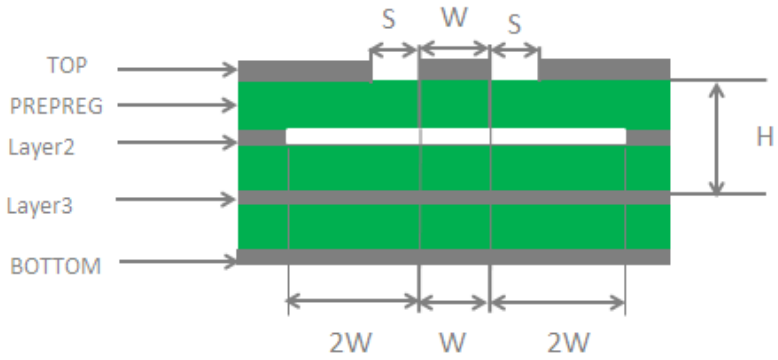


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

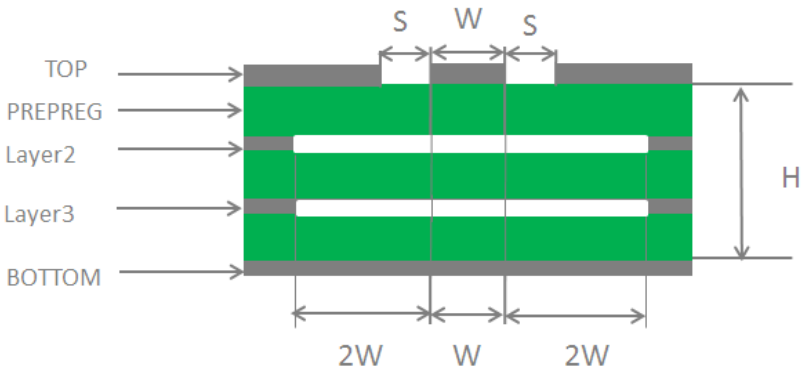


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

5.4. Antenna Installation

5.4.1. Antenna Design Requirements

Table 33: Antenna Design Requirements

Antenna Type	Requirements
GNSS [13]	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connectors provided by *HIROSE*.

[13] It is recommended to use a passive GNSS antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

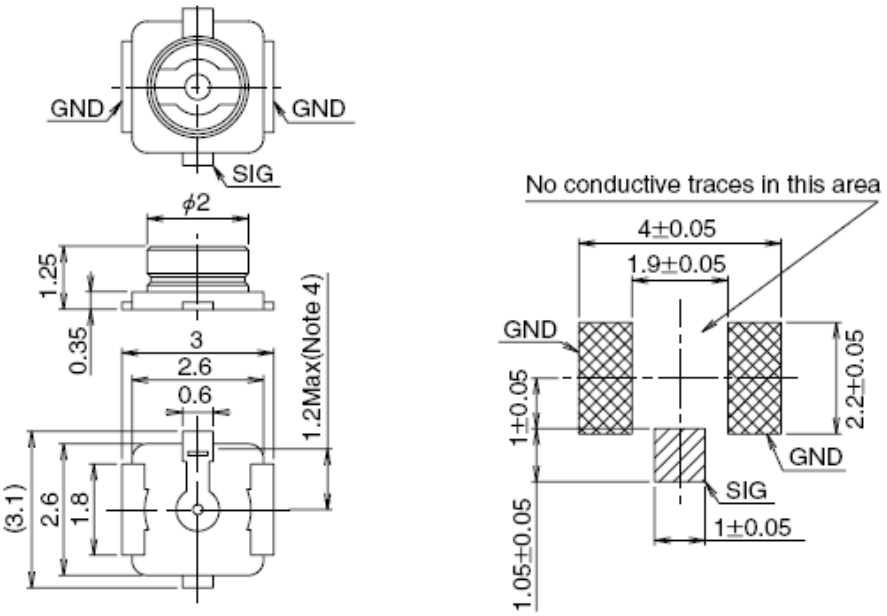


Figure 31: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

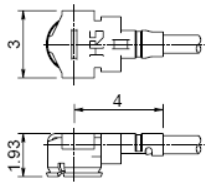
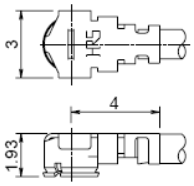
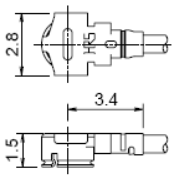
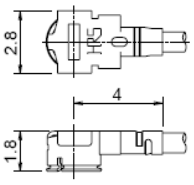
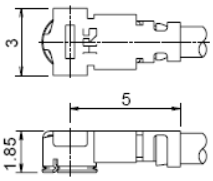
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 32: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connectors.

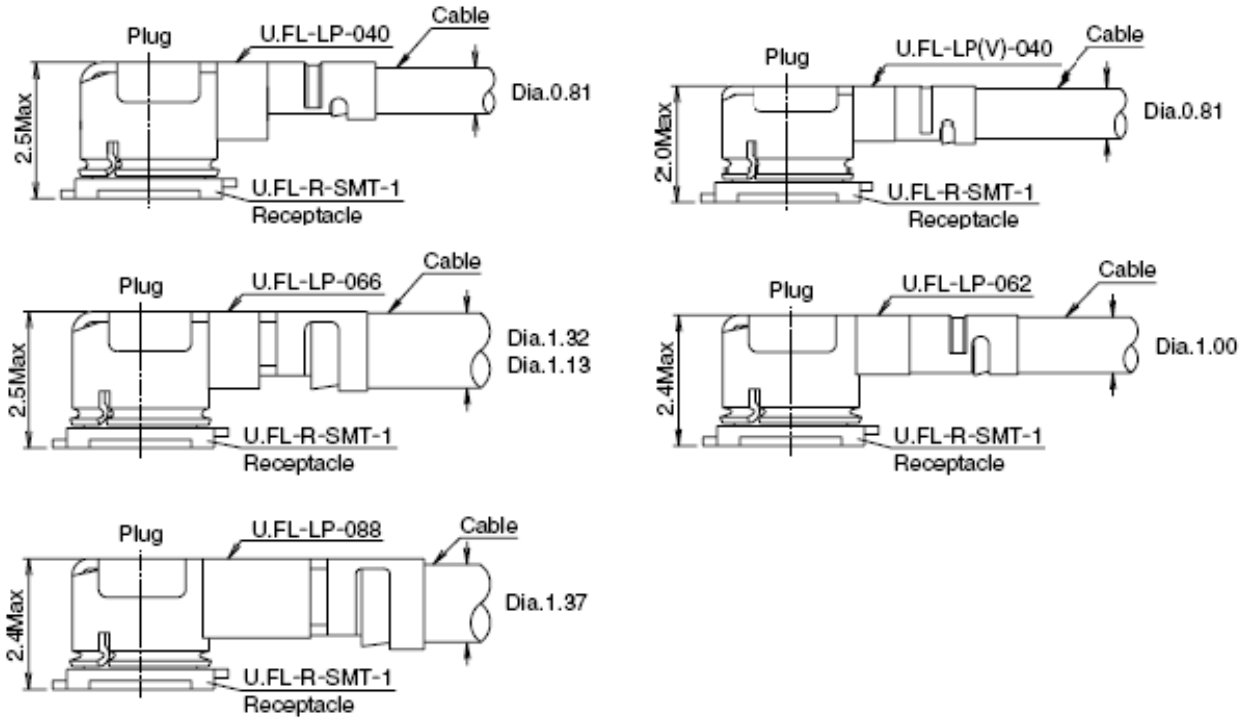


Figure 33: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Reliability, Radio and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 34: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6.0	V
USB_VBUS	1.3	1.8	V
Voltage at Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 35: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT [14]	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	2.6	3.3	4.8	V

[14] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

$I_{VBAT(peak)}$	Peak current of power supply in LTE Cat M1 and/or Cat NB2 transmission modes.	-	-	0.7	-	A
USBPHY_3P3	Power supply for USB PHY circuit	-	-	3.3	-	V
USB_VBUS	USB connection detection	-	1.3		1.8	V

6.3. Operating and Storage Temperatures

Table 36: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [15]	-35	+25	+75	ºC
Extended Temperature Range [16]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

6.4. Power Consumption

Table 37: BG77 Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Peak	Unit
Leakage [17]	Power-off @ USB/UART disconnected	12.08	-	μA
PSM	PSM @ USB/UART disconnected	3.44	-	μA
Rock Bottom	**AT+CFUN=0** @ Sleep mode	0.508	-	mA

[15] Within the operating temperature range, the module meets 3GPP specifications.
[16] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[17] The power consumption of the module in PSM is much lower than that in power off mode, due to the following two designs:

- More internal power supplies are powered off in PSM.
- Also the internal clock frequency is reduced in PSM.

Sleep Mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	1.61	-	mA
	LTE Cat NB1 DRX = 1.28 s	1.55	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.67	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.66	-	mA
Idle Mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	19.7	-	mA
	LTE Cat NB1 DRX = 1.28 s	15.8	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	19.3	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	15.4	-	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE-FDD B1 @ 21.16 dBm	200.82	501.25	mA
	LTE-FDD B2 @ 21.19 dBm	202.92	503.99	mA
	LTE-FDD B3 @ 21.33 dBm	213.12	540.04	mA
	LTE-FDD B4 @ 21.02 dBm	207.64	520.04	mA
	LTE-FDD B5 @ 21.22 dBm	226.22	576	mA
	LTE-FDD B8 @ 21.01 dBm	223	571.84	mA
	LTE-FDD B12 @ 21 dBm	197.21	478.2	mA
	LTE-FDD B13 @ 21.04 dBm	225.04	587.92	mA
	LTE-FDD B18 @ 21.08 dBm	222.29	571.45	mA
	LTE-FDD B19 @ 21 dBm	224.94	578.95	mA
	LTE-FDD B20 @ 21.02 dBm	227.94	600.21	mA
	LTE-FDD B25 @ 20.94 dBm	200.43	491.99	mA
	LTE-FDD B26 @ 20.93 dBm	219.87	564.15	mA
	LTE-FDD B27 @ 21.01 dBm	220.85	561.24	mA
	LTE-FDD B28A @ 21.07 dBm	201.87	500.59	mA

	LTE-FDD B28B @ 20.94 dBm	207.73	522.95	mA
	LTE-FDD B66 @ 20.98 dBm	207.66	514.61	mA
	LTE-FDD B85 @ 21.15 dBm	TBD	TBD	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE-FDD B1 @ 21.33 dBm	152.28	439.42	mA
	LTE-FDD B2 @ 21.48 dBm	158.09	469.09	mA
	LTE-FDD B3 @ 21.47 dBm	169.07	500.97	mA
	LTE-FDD B4 @ 21.05 dBm	158.28	474.84	mA
	LTE-FDD B5 @ 21.07 dBm	185.37	556.84	mA
	LTE-FDD B8 @ 20.98 dBm	177.76	530.27	mA
	LTE-FDD B12 @ 21.15 dBm	148.13	431.58	mA
	LTE-FDD B13 @21.14 dBm	186.86	562.81	mA
	LTE-FDD B18 @ 21.09 dBm	182.28	550.22	mA
	LTE-FDD B19 @ 21 dBm	182.93	548.13	mA
	LTE-FDD B20 @ 21.13 dBm	188.39	562.8	mA
	LTE-FDD B25 @ 21.43 dBm	158.35	464.47	mA
	LTE-FDD B28 @ 21.12 dBm	149.04	437.16	mA
	LTE-FDD B66 @ 21.34 dBm	164.84	488.87	mA
	LTE-FDD B71 @ 21.39 dBm	146.52	426.93	mA
	LTE-FDD B85 @ 21.35 dBm	TBD	TBD	mA

Table 38: GNSS Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold start @ instrument	78.23	mA
	Hot start @ instrument	78.73	mA
	Warm start @ instrument	77.45	mA
	Lost state @ instrument	77.71	mA

Tracking (**AT+CFUN=0**)	Instrument environment @ passive antenna	24.59	mA
	Open sky @ real network, passive antenna	21.15	mA
	Open sky @ real network, active antenna	24.14	mA

6.5. Tx Power

Table 39: BG77 RF Output Power

Frequency	Max. Tx Power	Min. Tx Power
LTE-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/ B26 [18]/B27 [18] /B28/B66/B71 [19]/B85	21 dBm +1.7/-3 dB	< -39 dBm

6.6. Rx Sensitivity

Table 40: BG77 Conducted RF Receiving Sensitivity

Band	Primary	Diversity	Receiving Sensitivity (dBm)	
			Cat M1/3GPP	Cat NB2 [20]/ 3GPP
LTE-FDD B1	Supported	-	-106.4/-102.3	-114/-107.5
LTE-FDD B2			-106.4/-100.3	-114.5/-107.5
LTE-FDD B3			-106/-99.3	-115/-107.5
LTE-FDD B4			-106/-102.3	-114/-107.5
LTE-FDD B5			-104/-100.8	-114/-107.5
LTE-FDD B8			-106/-99.8	-115.5/-107.5
LTE-FDD B12			-105.5/-99.3	-115/-107.5

[18] LTE-FDD B27 and B26 are supported by LTE Cat M1 only.
[19] LTE-FDD B71 is supported by LTE Cat NB2 only.
[20] LTE Cat NB2 receiving sensitivity without repetitions.

LTE-FDD B13	-105.5/-99.3	-115/-107.5
LTE-FDD B18	-105.5/-102.3	-115.5/-107.5
LTE-FDD B19	-106/-102.3	-115.5/-107.5
LTE-FDD B20	-107/-99.8	-115/-107.5
LTE-FDD B25	-107.5/-100.3	-114/-107.5
LTE-FDD B26	-106.5/-100.3	-
LTE-FDD B27	-107/-100.8	-
LTE-FDD B28	-106/-100.8	-115/-107.5
LTE-FDD B66	-106/-101.8	-115/-107.5
LTE-FDD B71	-	-114/-107.5
LTE-FDD B85	TBD/-100	TBD/-107.5

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

Table 41: Electrostatic Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±10	kV
Main/GNSS Antenna Interfaces	±5	±10	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

Figure 34: Module Top and Side Dimensions

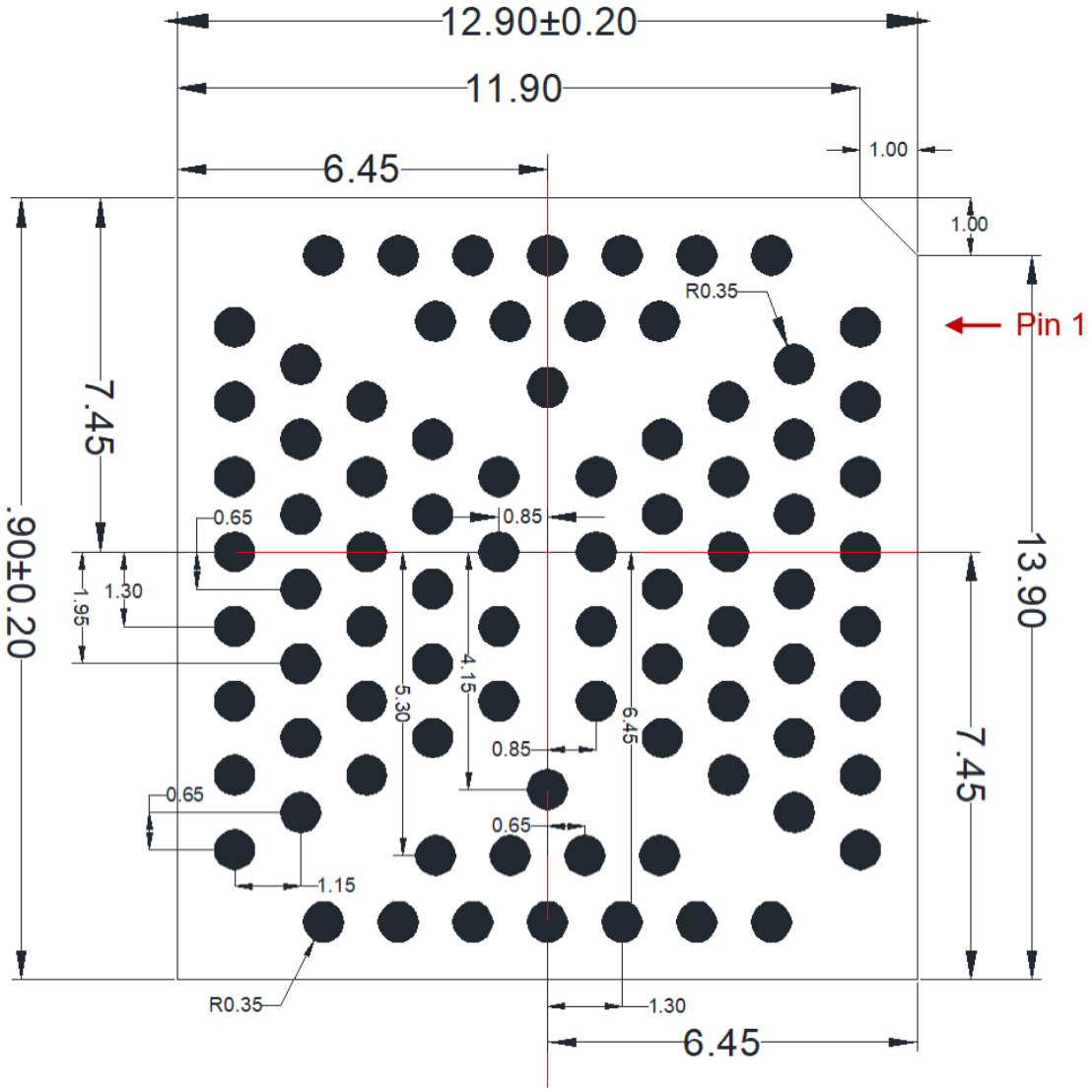


Figure 35: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

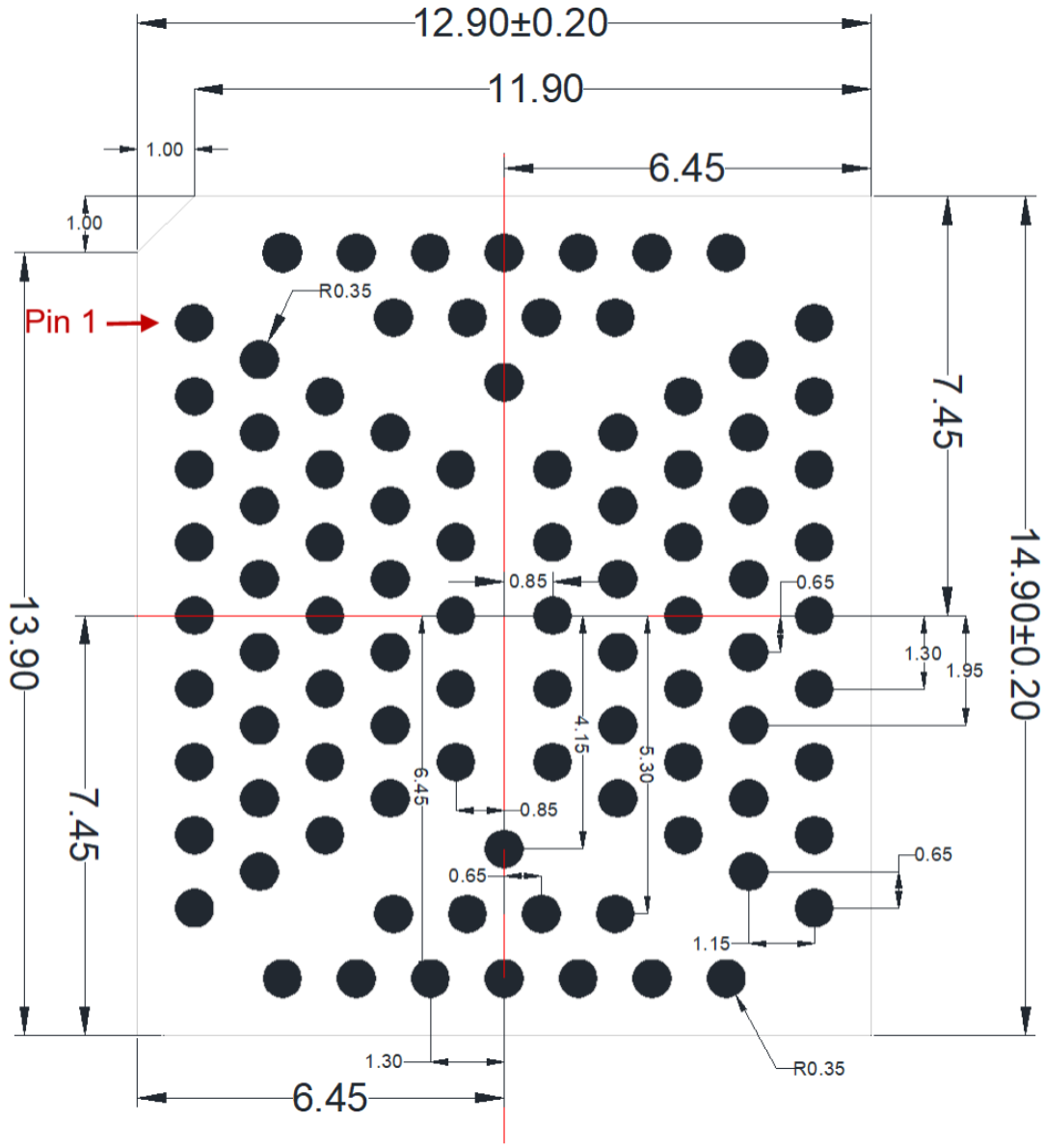


Figure 36: Recommended Footprint (Top View)

NOTE

1. For easy maintenance of the module, keep a distance of about 3 mm between the module and other components on the motherboard.
2. All reserved pins must be kept open.
3. For stencil design requirements of the module, see ***document [5]***.

7.3. Top and Bottom Views

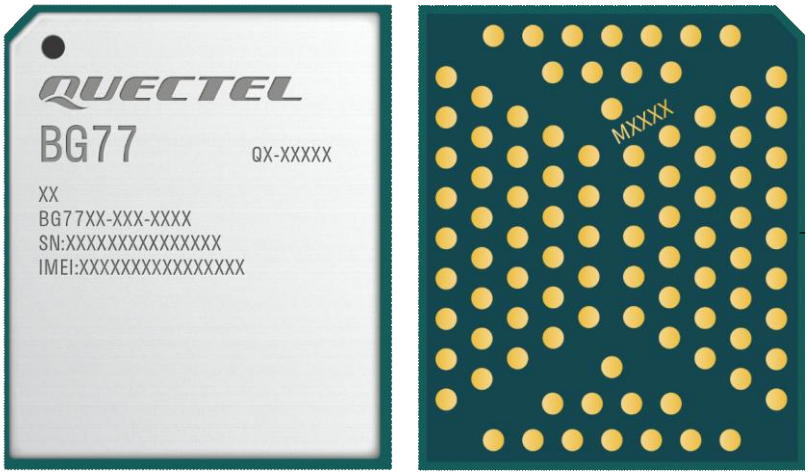


Figure 37: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [21] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[21] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.10–0.12 mm. For more details, see ***document [5]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

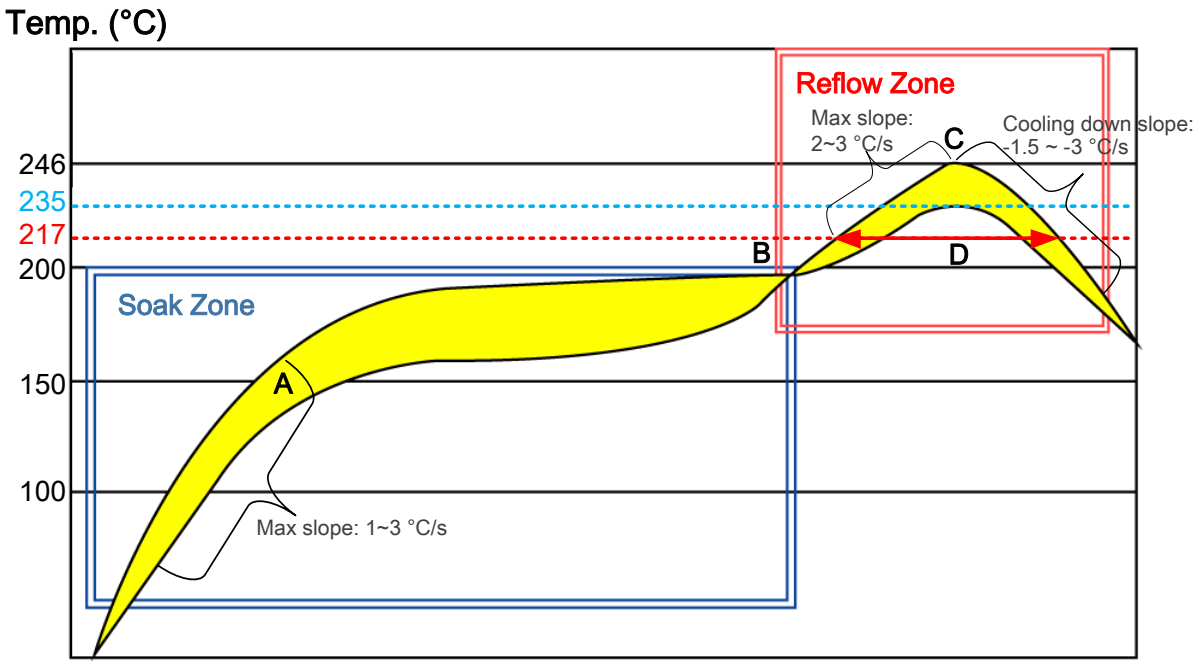


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 42: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

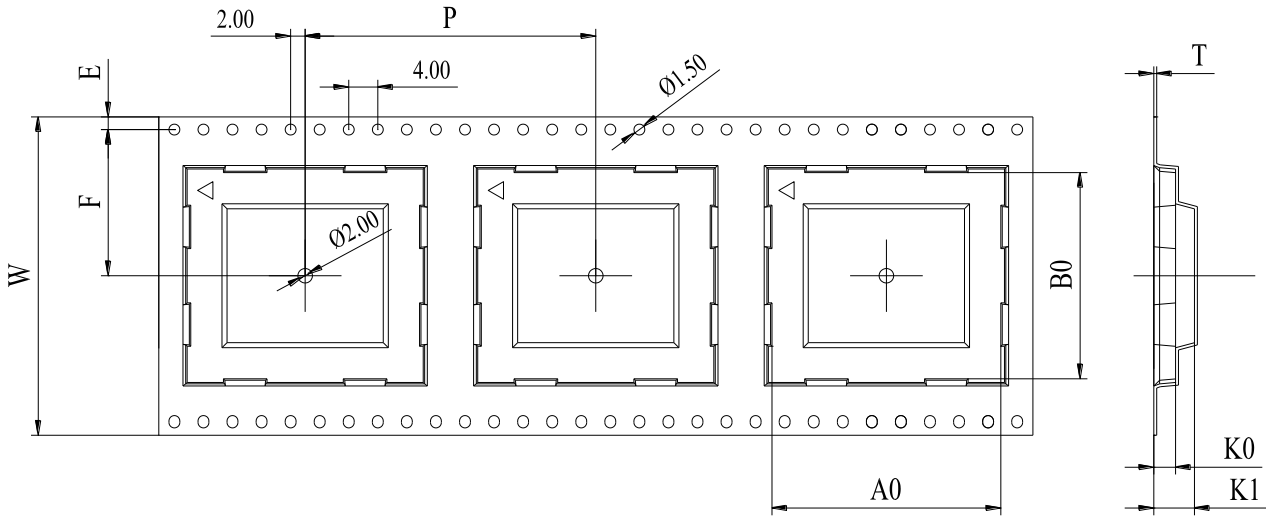


Figure 39: Carrier Tape Dimension Drawing

Table 43: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	20	0.35	13.3	15.3	2.35	5.35	14.2	1.75

8.3.2. Plastic Reel

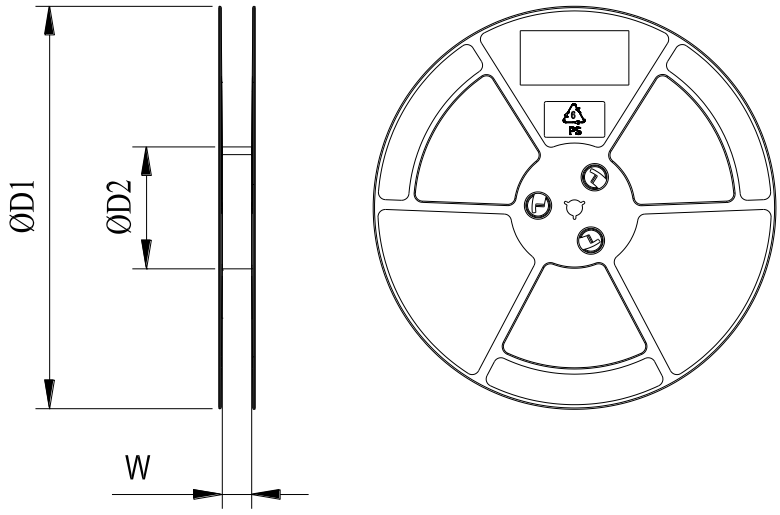
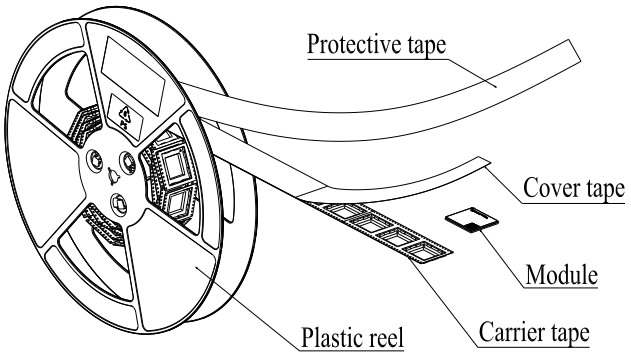


Figure 40: Plastic Reel Dimension Drawing

Table 44: Plastic Reel Dimension Table (Unit: mm)

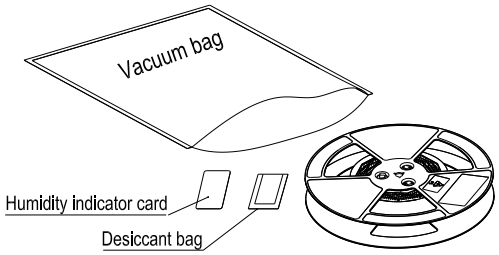
øD1	øD2	W
330	100	32.5

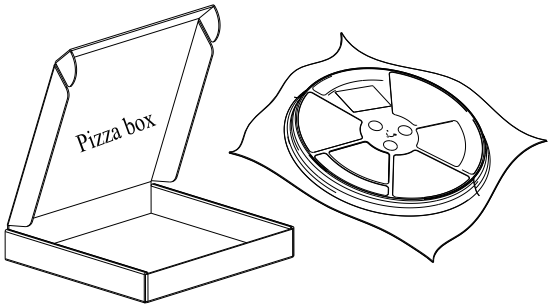
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 2000 modules.

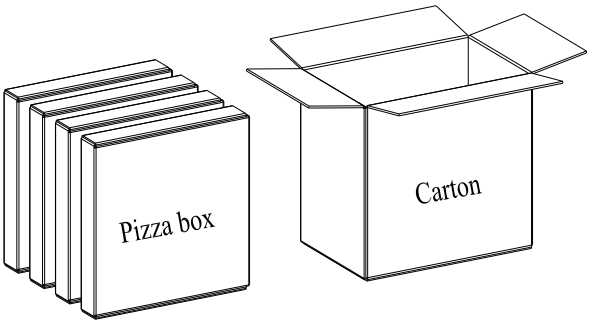


Figure 41: Packaging Process

9 Appendix A References

Table 45: Related Documents

Document Name
[1] Quectel_BG95&BG77&BG600L_Series_GNSS_Application_Note
[2] Quectel_UMTS&LTE_EVB_User_Guide
[3] Quectel_BG95&BG77&BG600L_Series_AT_Commands_Manual
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Secondary_SMT_Application_Note
[6] Quectel_BG95&BG77&BG600L_Series_QCFG_AT_Commands_Manual

Table 46: Terms and Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CoAP	Constrained Application Protocol
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DRX	Discontinuous Reception
EGSM	Extended GSM (Global System for Mobile Communications)
e-I-DRX	Extended Idle Mode Discontinuous Reception

EPC	Evolved Packet Core
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FTP(S)	File Transfer Protocol Secure
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	Generic RF controller
HSS	Home Subscriber Server
HTTP(S)	Hypertext Transfer Protocol Secure
I2C	Inter-Integrated Circuit
I/O	Input/Output
IoT	Internet of Things
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low-Power Wide-Area
LTE	Long Term Evolution
LwM2M	Lightweight M2M
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
MT	Mobile Terminated

NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
Rx	Receive
RHCP	Right Hand Circularly Polarized
RTS	Request to Send
SAW	Surface Acoustic Wave
SMD	Surface Mount Device
SMS	Short Message Service
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDM	Time-Division Multiplexing
TLS	Transport Layer Security
TVS	Transient Voltage Suppressor
UDP	User Datagram Protocol

UE	User Equipment
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VoLTE	Voice (voice calls) over LTE
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network

10 Appendix B Compulsory Certifications

By the issue date of the document, BG77 has been certified by JATE and TELEC.

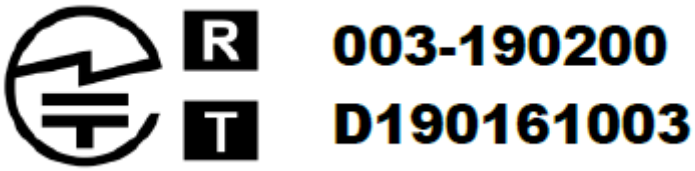


Figure 42: JATE/TELEC Certification ID