RM500Q-GL

Hardware Design

5G Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2020-08-31	Norton ZHANG/ Kingson ZHANG Qiqi WANG	Initial
1.1	2021-03-10	Norton ZHANG Jerax KONG	1. Updated the status of 5G NR SA bands (in Table 2); 2. Added the supported GNSS system: GZSS (in Table 2); 3. Updated application fields of the module (in Chapter 2.1); 4. Updated the content and notes of key features (Chapter 2.2); 5. Updated 5G NR features (in Table 3); 6. Updated the temperature range of the module; 7. Updated I/O parameter definitions and deleted M.2 Socket 2 PCIe-based Pinout descriptions (in Chapter 2.6); 8. Updated the description of turn-on/turn-off/reset timing and PCIe timing of the module (in Chapter 3.4, Chapter 3.5, Chapter 3.6 and Chapter 4.3.4); 9. Updated the content of (U)SIM interfaces (Chapter 4.1); 10. Updated MIMO1 to PRX MIMO, and MIMO2 to DRX MIMO (in Chapter 5); 11. Updated WCDMA information of ANT0 and ANT3 (in Table 30 and Table 31); 12. Updated 5G NR receiving sensitivity data (Table 33); 13. Added new chapters: Chapter 1.2, Chapter 1.3, Chapter 5.3.4, and Chapter 5.3.5; 14. Updated current consumption data (Table 40); 15. Updated the reference image of the module (Figure 38).

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1 Introduction

1.1. Introduction

This document introduces RM500Q-GL module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate its application in different fields, reference design is also provided for reference. Coupled with application notes and user guides, you can easily design and set up mobile applications with RM500Q-GL. You can also view the RM500Q-GL reference design to understand the module hardware architecture. For details, see ***document [1]***.

1.2. Reference Standard

The module complies with the following standards:

- *PCI Express M.2 Specification Revision 3.0, Version 1.2*
- *PCI Express Base Specification Revision 3.0*
- *Universal Serial Bus 3.1 Specification*
- *ISO/IEC 7816-3*
- *MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
- *3GPP TS 27.007* and *3GPP TS 27.005*

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, ANTCTL[1:2] refers to both two ANTCTL pins, ANTCTL1 and ANTCTL2.

2 Product Concept

2.1. General Description

RM500Q-GL is a 5G NR/LTE-FDD/LTE-TDD/UMTS/HSPA+ wireless communication module with receive diversity. It provides data connectivity on 5G NR SA and NSA, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks. RM500Q-GL is standard M.2 Key-B WWAN module. For more details, see *PCI Express M.2 Specification Revision 3.0, Version 1.2*.

RM500Q-GL is an industrial-grade module for industrial and commercial applications only.

RM500Q-GL supports embedded operating systems such as Windows, Linux and Android, and also provides GNSS and voice functionality to meet specific application demands.

The following table shows the frequency bands and GNSS systems of RM500Q-GL module.

Table 2: Frequency Bands and GNSS Systems of RM500Q-GL Module

Mode	RM500Q-GL
5G NR SA	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48*/n66/n71/n77/n78/n79
5G NR NSA	n38/n41/n77/n78/n79
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71
LTE-TDD	B34/B38/B39/B40/B41/B42/B43/B48
LAA	B46
WCDMA	B1/B2/B3/B4/B5/B8/B19
GNSS	GPS/GLONASS/BeiDou(COMPASS)/Galileo/QZSS

RM500Q-GL can be applied in the following fields:

- Rugged tablet PC and laptop computer
- Remote monitor system
- Smart metering system
- Wireless CPE
- Smart TV
- Outdoor Live devices
- Wireless router and switch
- Other wireless terminal devices

2.2. Key Features

The following table describes key features of RM500Q-GL.

Table 3: Key Features of RM500Q-GL

Feature	Details
Function Interface	● PCI Express M.2 Interface
Power Supply	● Supply voltage: 3.135–4.4 V ● Typical supply voltage: 3.7 V
(U)SIM Interface	● Compliant with *ISO/IEC 7816-3* ● Supported (U)SIM card: Class B (3.0 V) and Class C (1.8 V) ● (U)SIM1 and (U)SIM2 interfaces ● Dual SIM Single Standby
USB Interface	● Compliant with USB 3.1 and 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice over USB. ● Supported USB serial drivers: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x/10
PCIe Interface	● Complaint with PCIe Gen 3 ● PCIe × 1, supporting 8 Gbps per lane. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output
PCM Interface	● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but must be the master in long frame

	synchronization
Transmitting Power	● WCDMA bands: Class 3 (24 dBm +1/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE B38/B40/B41/B42/B43 bands HPUE [1]: Class 2 (26 dBm ±2 dB) ● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR n41/n77/n78/n79 bands HPUE: Class 2 (26 dBm +2/-3 dB)
5G NR Features	● Supports 3GPP Rel-15 ● Supported modulations: - Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supported MIMO: - Uplink: 2 × 2 MIMO [2] on n41/n77/n78/n79 - Downlink: 4 × 4 MIMO on n1/n2/n3/n7/25/n38/n40/n41/n48*/n66/n77/ n78/n79 ● SCS 15 kHz [3] and 30 kHz [3] ● SA and NSA operation modes [4] - NSA on n38/n41/n77/n78/n79 - SA on all the 5G bands ● Option 3x, 3a, 3, and Option 2 ● Max. transmission data rates [5] - NSA: 2.5 Gbps (DL)/ 650 Mbps (UL) - SA: 2.1 Gbps (DL)/ 900 Mbps (UL)
LTE Features	● Supports 3GPP Rel-15 ● LTE Category: DL Cat 16; UL Cat 18 ● Supported Modulations: - Uplink QPSK, 16QAM, 64QAM and 256QAM* - Downlink QPSK, 16QAM, 64QAM and 256QAM ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports DL 4 × 4 MIMO on: B1/B2/B3/B4/B7/B25/B30/B32/B34/B38/B39/B40/B41/B42/B43/B48/B66 ● Max. transmission data rates [5]: 1.0 Gbps (DL)/ 200 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulations ● Max. transmission data rates [5]: - DC-HSDPA: 42 Mbps (DL) - HSUPA: 5.76 Mbps (UL) - WCDMA: 384 kbps (DL/UL)
Rx-diversity	● 5G NR/LTE/WCDMA Rx-diversity
GNSS Features	● Qualcomm Gen9C Lite ● Protocol: NMEA 0183 ● Data Update Rate: 1 Hz
Antenna	● ANT0, ANT1, ANT2_GNSSL1, and ANT3

Interfaces	
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Internet Protocol Features	● Supports QMI/NTP* protocols ● Supports the protocols PAP and CHAP usually used for PPP connections
Firmware Upgrade	● USB 2.0 interface ● PCIe interface ● DFOTA
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
Physical Characteristics	● M.2 Key-B ● Size: (30.0 ±0.15) mm × (52.0 ±0.15) mm × (2.3 ±0.2) mm ● Weight: approx. 8.7 g
Temperature Range	● Operating temperature range: -30 °C to +70 °C [6)] ● Extended temperature range: -40 °C to +85 °C [7)] ● Storage temperature range: -40°C to +90°C
RoHS	● All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] HPUE is only for single carrier.
2. [2)] Uplink 2 × 2 MIMO is only supported in 5G SA mode.
3. [3)] 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.
4. [4)] See ***document [2]*** for bandwidth supported by each frequency band in the NSA and SA modes.
5. [5)] The maximum rates are theoretical and for the actual values, refer to the network configuration.
6. [6)] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
7. [7)] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.3. Evaluation Board

To help you develop applications conveniently with RM500Q-GL, Quectel supplies an evaluation board (PCIe Card EVB), a USB to RS-232 converter cable, a USB type-B cable, antennas and other peripherals to control or test the module. For more details, see ***document [3]***.

2.4. Functional Diagram

The following figure shows the functional diagram of RM500Q-GL.

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface

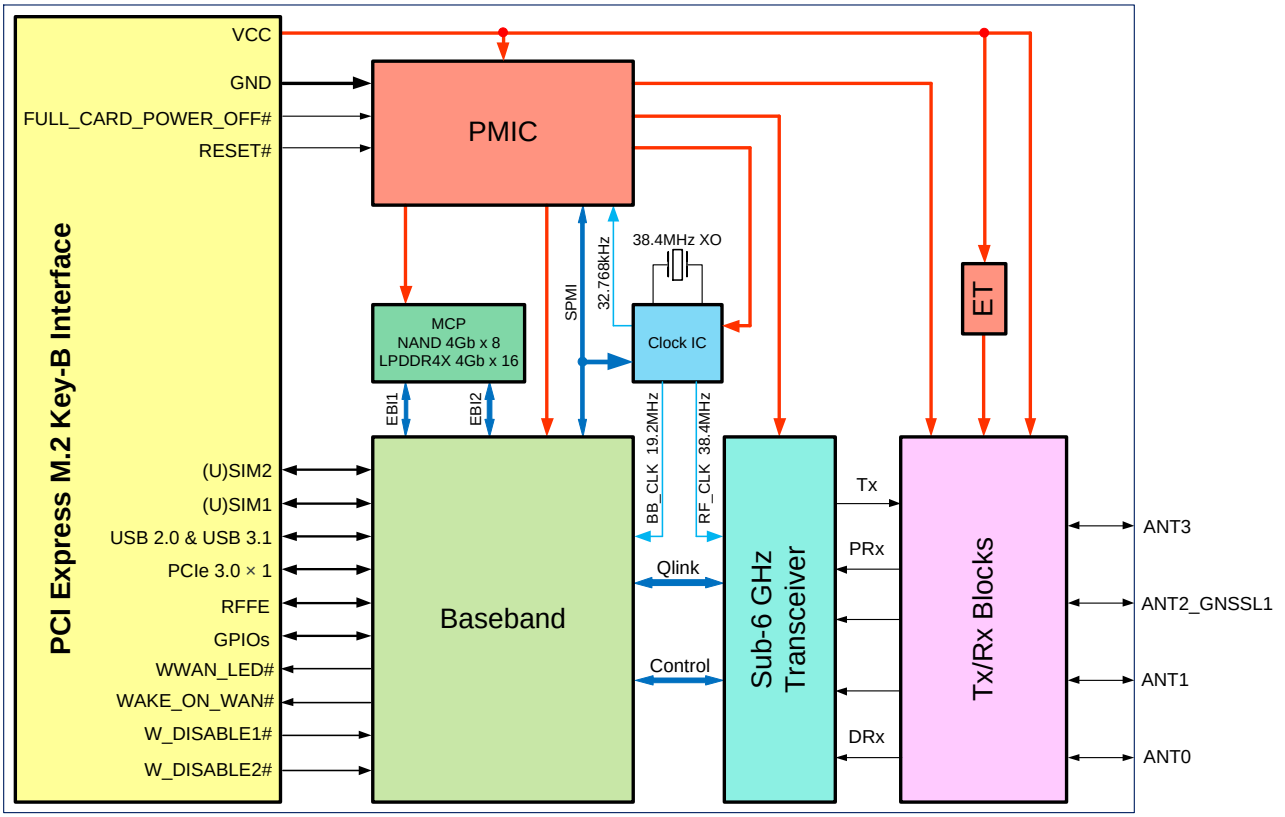
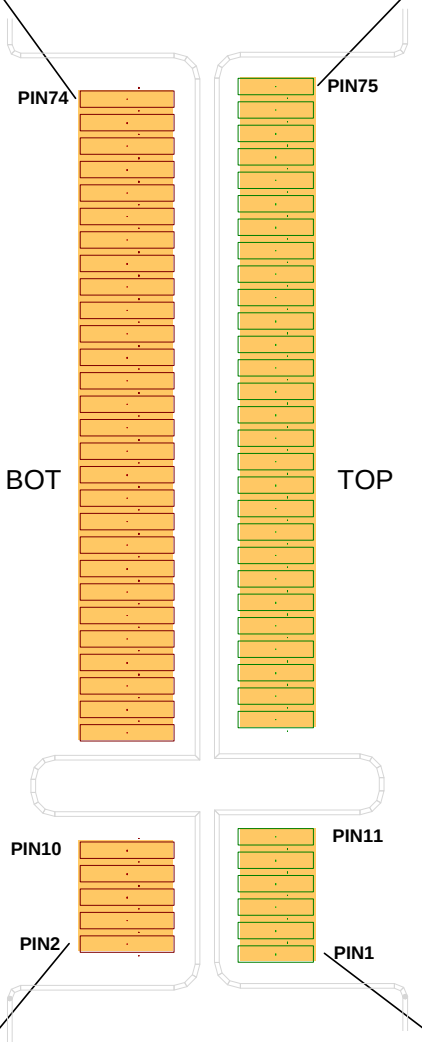


Figure 1: Functional Block Diagram

2.5. Pin Assignment

The following figure shows the pin assignment of RM500Q-GL. The top side contains the four antenna connectors.

No.	Pin Name
74	VCC
72	VCC
70	VCC
68	AP2SDX_STATUS
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	WLAN_TX_EN
58	RFFE_DATA
56	RFFE_CLK
54	PCIE_WAKE_N
52	PCIE_CLKREQ_N
50	PCIE_RST_N
48	USIM2_VDD
46	USIM2_RST
44	USIM2_CLK
42	USIM2_DATA
40	USIM2_DET
38	SDX2AP_STATUS
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	PCM_SYNC
26	W_DISABLE2#
24	PCM_DOUT
22	PCM_DIN
20	PCM_CLK
	Notch
	Notch
	Notch
	Notch
10	WWAN_LED#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC



Pin Name	No.
CONFIG_2	75
GND	73
GND	71
CONFIG_1	69
RESET#	67
RFFE_VIO_1V8	65
ANTCTL2	63
ANTCTL1	61
LAA_TX_EN	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment

2.6. Pin Description

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down

The following table shows the pin definition and description of RM500Q-GL.

Table 5: Pin Description

PIN No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V	

5	GND		Ground		
6	FULL_CARD_ POWER_OFF#	DI	Turn on/off of the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Internally pulled down with a 100 kΩ resistor
7	USB_DP	AIO	USB 2.0 differential data (+)		
8	W_DISABLE1#	DI, OD	Airplane mode control. Active LOW.	1.8/3.3 V	
9	USB_DM	AIO	USB 2.0 differential data (-)		
10	WWAN_LED#	DO, OD	RF status indication LED Active LOW		
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V	
21	CONFIG_0	DO	Not connected internally		
22	PCM_DIN	DI	PCM data input	1.8 V	
23	WAKE_ON_WAN#	DO, OD	Wake up the host. Active LOW	1.8/3.3 V	
24	PCM_DOUT	DO, PD	PCM data output	1.8 V	
25	DPR*	DI, PU	Dynamic power reduction. High level by default	1.8 V	

26	W_DISABLE2#	DI, OD	GNSS disable control. Active LOW	1.8/3.3 V
27	GND		Ground	
28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
33	GND		Ground	
34	USIM1_DATA	DIO, PU	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	USIM1_VDD 1.8/3.0 V
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)	
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
39	GND		Ground	
40	USIM2_DET [1)]	DI, PU	(U)SIM2 card insertion detection	1.8 V
41	PCIE_TX_M	AO	PCIe transmit (-)	
42	USIM2_DATA	DIO, PU	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V
43	PCIE_TX_P	AO	PCIe transmit (+)	
44	USIM2_CLK	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
45	GND		Ground	
46	USIM2_RST	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
47	PCIE_RX_M	AI	PCIe receive (-)	
48	USIM2_VDD	PO	Power supply for	USIM2_VDD

			(U)SIM2 card	1.8/3.0 V	
49	PCIE_RX_P	AI	PCIe receive (+)		
50	PCIE_RST_N	DI, OD	PCIe reset. Active LOW		
51	GND		Ground		
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW.		
53	PCIE_REFCLK_M	AI, AO	PCIe reference clock (-)		
54	PCIE_WAKE_N	DO, OD	PCIe wake up. Active LOW		
55	PCIE_REFCLK_P	AI, AO	PCIe reference clock (+)		
56	RFFE_CLK [2)]	DO, PD	Used for external MIPI IC control	1.8 V	
57	GND		Ground		
58	RFFE_DATA [2)]	DO, PD	Used for external MIPI IC control	1.8 V	
59	LAA_TX_EN*	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V	
60	WLAN_TX_EN*	DI	Notification from WLAN to SDR while transmitting	1.8 V	
61	ANTCTL1 *	DO, PD	Antenna GPIO control	1.8 V	
62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive data	1.8 V	
63	ANTCTL2*	DO, PD	Antenna GPIO control	1.8 V	
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit	1.8 V	
65	RFFE_VIO_1V8 [2)]	PO	Power supply for antenna tuner	1.8 V	Maximum output current: 50 mA
66	USIM1_DET [1)]	DI, PU	(U)SIM1 card insertion detection	1.8 V	
67	RESET#	DI	Reset the module. Active LOW	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V with a 100 kΩ resistor
68	AP2SDX_STATUS*	DI	Status indication from AP	1.8 V	

69	CONFIG_1	DO	Connected to GND internally	
70	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
71	GND		Ground	
72	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
73	GND		Ground	
74	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
75	CONFIG_2	DO	Not connected internally	

NOTES

1. [1)] This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.
2. [2)] If this function is required, please contact Quectel for more details.
3. Keep all NC, reserved and unused pins unconnected.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes to be mentioned in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network is connected. In this mode, the power consumption is determined by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE1# pin LOW will set the module to airplane mode. In this mode, the RF function is invalid.	
Sleep Mode	The module keeps receiving paging messages, SMS, voice calls and TCP/UDP data from the network with its current consumption reducing to the minimal level.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VCC) remains applied.	

3.1.1. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during the sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

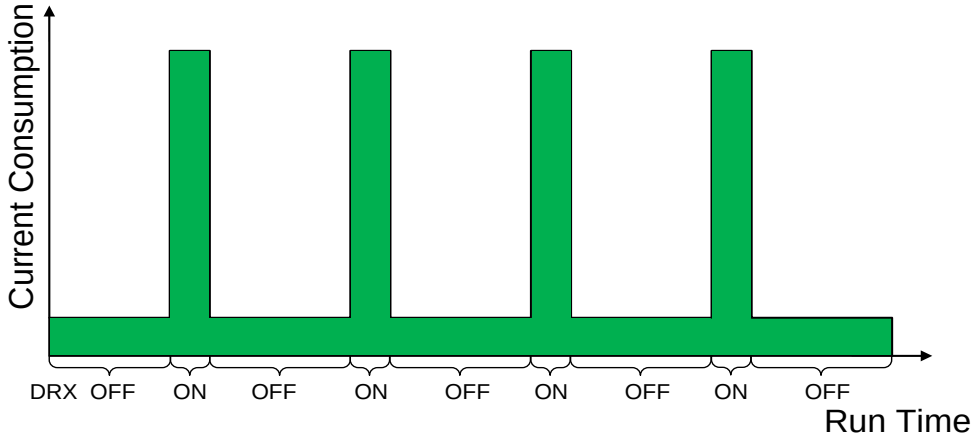


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following part of this section presents the power saving procedure and sleep mode of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to make the module enter sleep mode.

- **AT+QSCLK=1** command is executed to enable the sleep mode.
- Then the host's USB bus, which is connected to the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

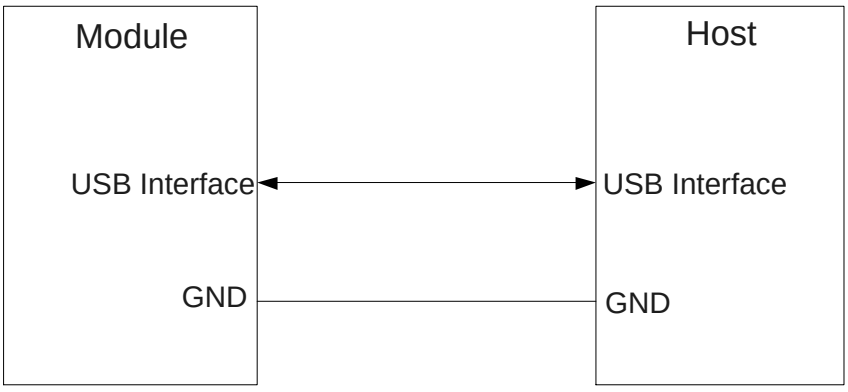


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions:

- Sending data to module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB bus to wake up the host.

3.1.2. Airplane Mode

The module provides a W_DISABLE1# pin to disable or enable the airplane mode through hardware operation. See ***Chapter 4.5.1*** for more details.

3.2. Communication Interface with a Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below:

USB Mode

- Supports all USB 2.0/3.1 features
- Supports MBIM/QMI/QRTR/AT
- Communication can be switched to PCIe mode by AT command

USB is the default communication interface between the module and the host. To use PCIe interface for the communication between a host, an AT command under USB mode can be used. For more details about the AT command, see ***document [4]***.

It is suggested that USB 2.0 interface be reserved for firmware upgrade.

USB-AT-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT
- Communication can be switched back to USB mode by AT command

When the module works at the USB-AT-based (switched from USB mode by AT command) PCIe mode, it supports MBIM/QMI/QRTR/AT, and can be switched back to USB mode by AT command. But the firmware upgrade via PCIe interface is not supported, so USB 2.0 interface must be reserved for the firmware upgrade.

eFuse-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT
- Supports Non-X86 systems and X86 system (supports BIOS PCIe early initial)

RM500Q-GL can also be reprogrammed to PCIe mode based on eFuse. If the communication is switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

Note that if the host does not support firmware upgrade through PCIe, the firmware can be upgraded by the PCIe Card EVB, which could be inserted into a PC. For more details, see ***document [3]***.

3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

Table 7: Definition of VCC and GND Pins

Pin No.	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power Supply	3.135–4.4 V 3.7 V typical DC supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND	-	Ground	-

3.3.1. Decrease Voltage Drop

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will be powered off automatically. The voltage ripple of the input power supply should to be less than 100 mV, and the maximum voltage drop should be less than 165 mV, as shown by the following figure.

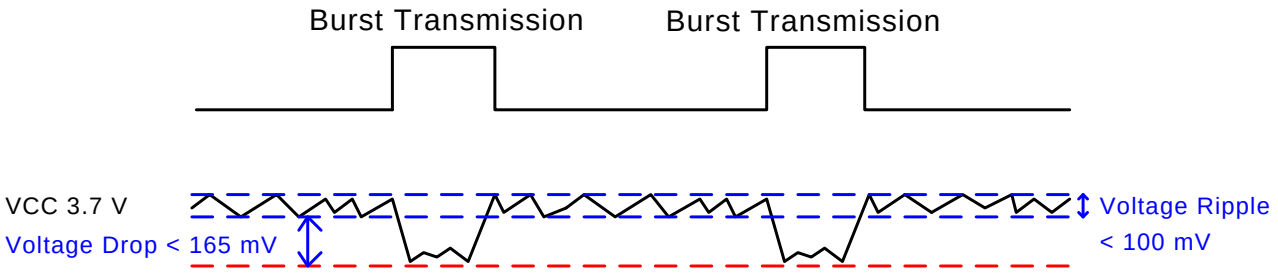


Figure 5: Power Supply Limits During Radio Transmission

Ensure the continuous current capability of the power supply is 3.0 A. To decrease the voltage drop, energy storage capacitors of about 220 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its ultra-low ESR. It is recommended to use four ceramic capacitors (1 µF, 100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be no less than 2.0 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to guarantee stability of the power supply, please use a zener diode with a reverse zener voltage of 5.1 V and a dissipation power of higher than 0.5 W. The following figure shows a reference circuit for the VCC.

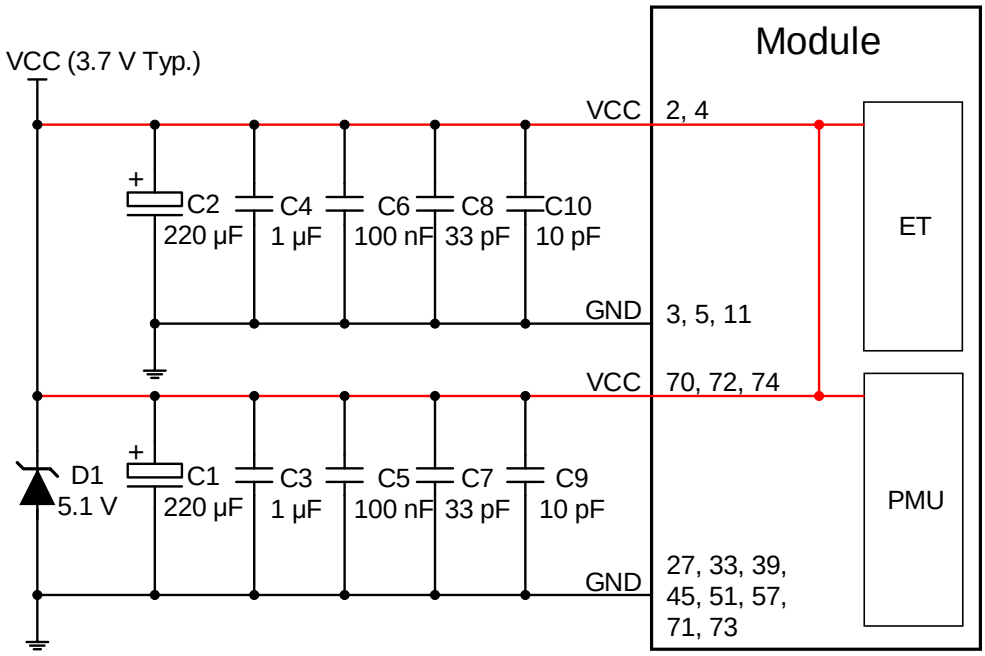


Figure 6: Reference Circuit for VCC Pins

3.3.2. Reference Design for Power Supply

Power design is critical as the module's performance largely depends on its power source. The power supply of the module should be able to provide a sufficient current of 3.0 A at least. If the voltage difference between input and output is not too big, use an LDO when supplying power to the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V typical), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5.0 V input power source based on the DC-DC converter. The typical output of the power supply is about 3.7 V and the maximum load current is 3.0 A.

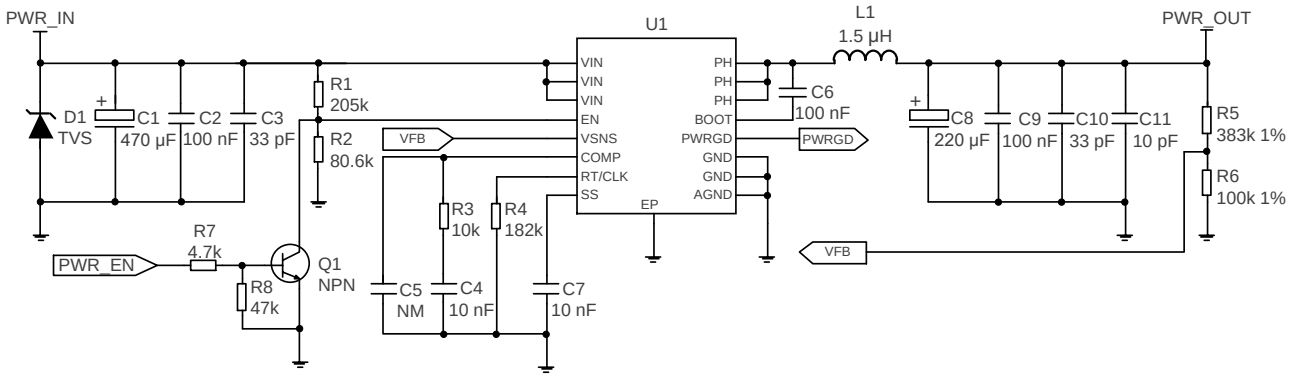


Figure 7: Reference Design for Power Supply

NOTE

To avoid damages to the internal flash, DON'T cut off the power supply before the module is completely turned off by pulling down FULL_CARD_POWER_OFF# pin for more than 7 s, and DON'T cut off power supply directly when the module is working.

3.3.3. Monitor the Power Supply

AT+CBC command can be used to monitor the voltage value of VCC. For more details, see ***document [4]***.

3.4. Turn on

FULL_CARD_POWER_OFF# (abbreviated as "FCPO#" in this document) is used to turn on/off the module. When the input signal is asserted HIGH (≥ 1.19 V), the module will turn on.

This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. And it has internally pulled down with a 100 kΩ resistor.

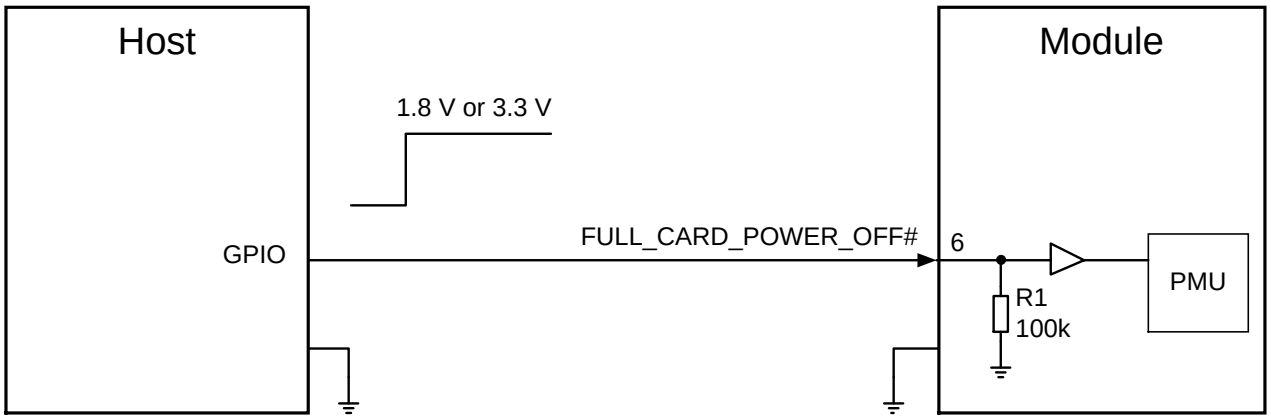
The following table shows the definition of FULL_CARD_POWER_OFF#.

.

Table 8: Definition of FCPO#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_ POWER_OFF#	DI, PD	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pull down with a 100 kΩ resistor

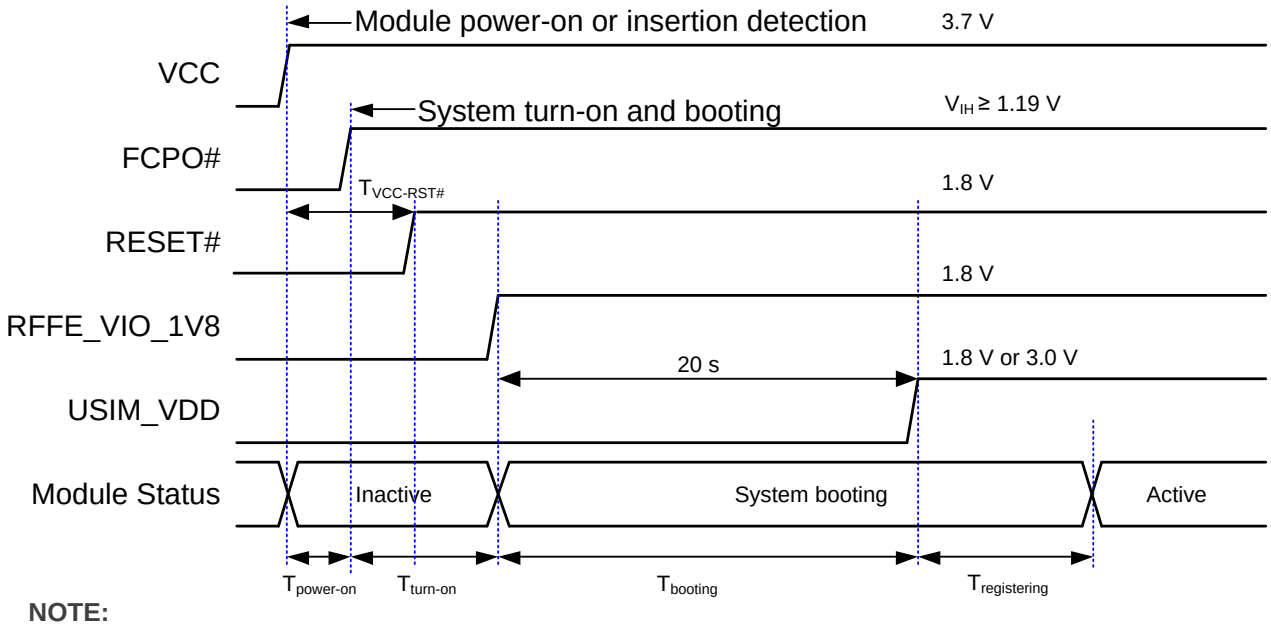
It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated by the following figure.



NOTE:
The voltage of pin 6 should be no less than 1.19 V when it is at high level.

Figure 8: Turn on the Module with a Host GPIO

The timing of turn-on scenario is illustrated by the following figure.



NOTE:
The host only needs to control FCPO#.

Figure 9: Turn-on Timing of the Module

Table 9: Turn-on Timing of the Module

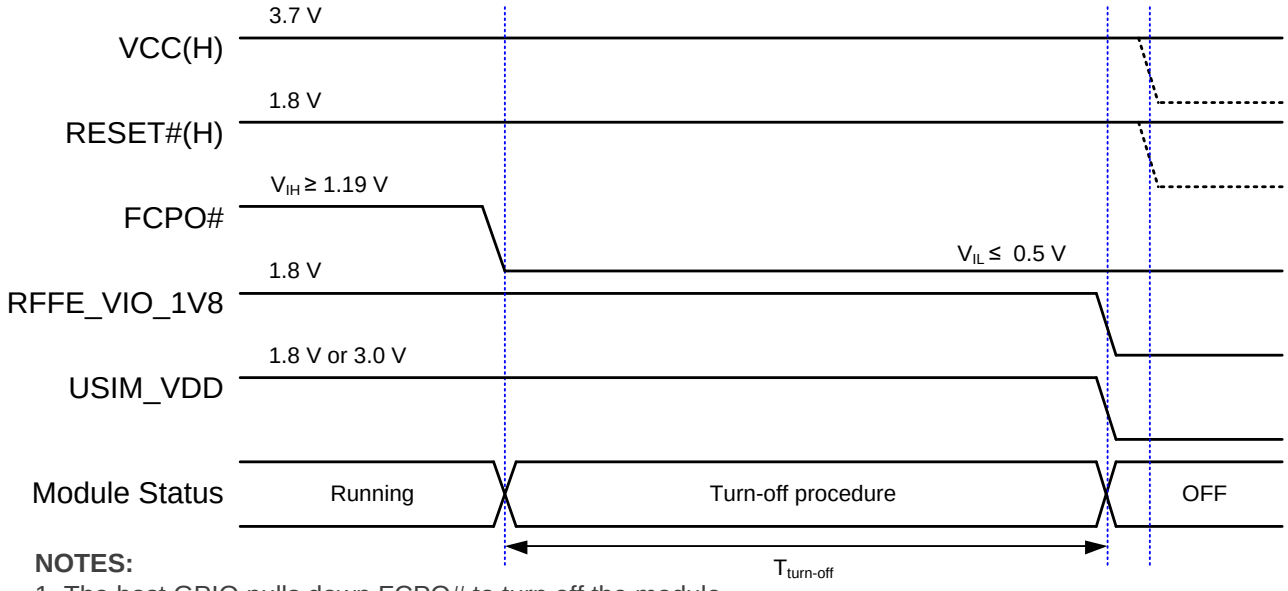
Symbol	Min.	Typ.	Max.	Comment
$T_{power-on}$	0 ms	20 ms	-	Module power-on time depending on the host.
$T_{VCC-RST\#}$	-	33 ms	-	Time period between module power-on and RESET# being driven HIGH.
$T_{turn-on}$	68 ms	-	-	Module system turn-on time.
$T_{booting}$	20 s	22 s	-	Module system booting time.
$T_{registering}$	-	-	-	Network registering time related to network CSQ.

3.5. Turn off

3.5.1. Turn off the Module Through FCPO#

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, driving FULL_CARD_POWER_OFF# pin LOW (≤ 0.2 V) or tri-stating the pin will turn off the module.

The timing of turning-off scenario is illustrated by the following figure.



NOTES:
1. The host GPIO pulls down FCPO# to turn off the module.
2. As shown by the dotted line, it is recommended to disconnect VCC and drive RESET# LOW after the

Figure 10: Turn-off Timing Through FCPO#

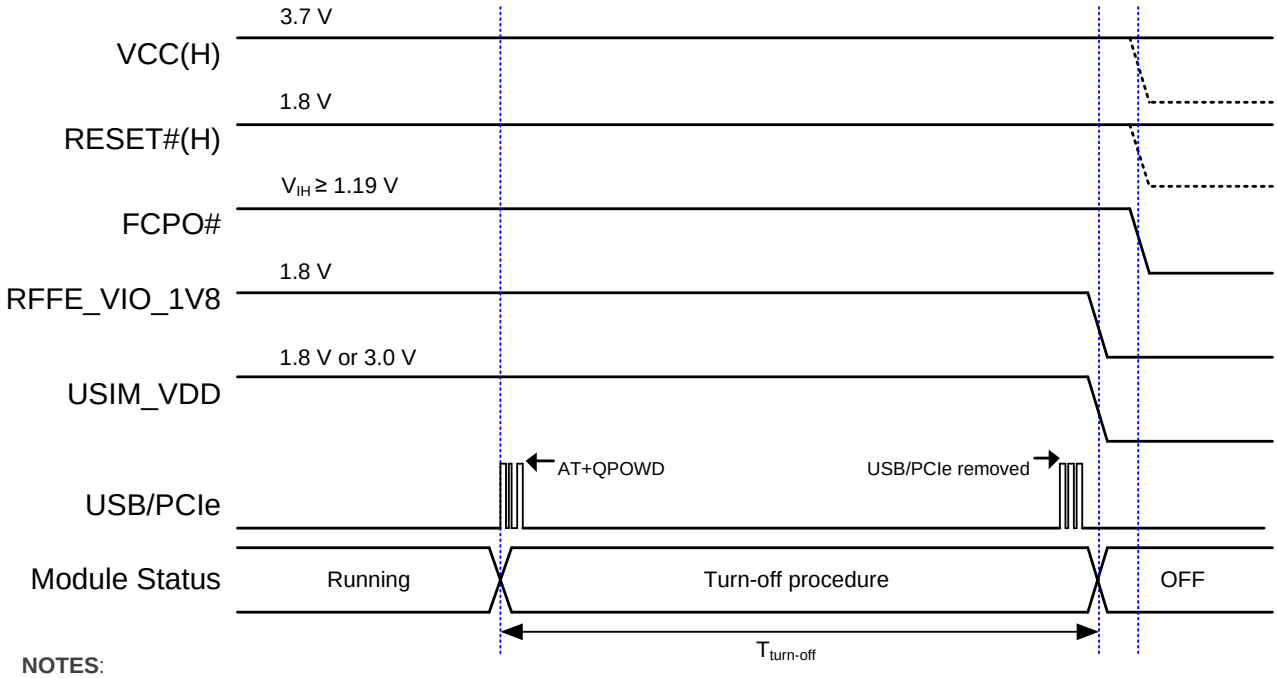
Table 10: Turn-off Timing of the Module Through FCPO#

Symbol	Min.	Typ.	Max.	Comment
$T_{turn-off}$	6.84s	-	-	Module system turn-off time.

3.5.2. Turn off the Module Through AT Command

It is also a safe method to turn off the module by **AT+QPOWD** command. For more details about the command, see ***document [4]***.

The module is designed to be turned on with a host GPIO. Pull down FULL_CARD_POWER_OFF# pin after the module's USB/PCIe is removed. Otherwise, the module will turn on again.



NOTES:
1. Please pull down FULL_CARD_POWER_OFF# pin immediately or cut off the power supply VCC when the host detects that the module USB/PCIe is removed.
2. It is recommended to cut off the VCC after the module is turned off and drive RESET# LOW after the module shuts down.

Figure 11: Turn-off Timing Through AT Command and FCPO#

Table 11: Turn-off Timing of the Module Through AT Command and FCPO#

Symbol	Min.	Typ.	Max.	Comment
$T_{turn-off}$	6.84 s	-	-	Module system turn-off time.

3.6. Reset the Module

RESET# is an asynchronous and active LOW signal (1.8 V logic level). Whenever this pin is active, the module will immediately enter Power On Reset (POR) condition.

Please note that triggering the RESET# signal will lead to loss of all data in the modem and removal of system drivers. It will also disconnect the modem from the network.

Table 12: Definition of RESET# Pin

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
67	RESET#	DI, PU	Reset the module Active LOW	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V with a 100 kΩ resistor

The module can be reset by pulling down the RESET# pin for 200–980 ms. An open collector/drain driver or button can be used to control the RESET# pin.

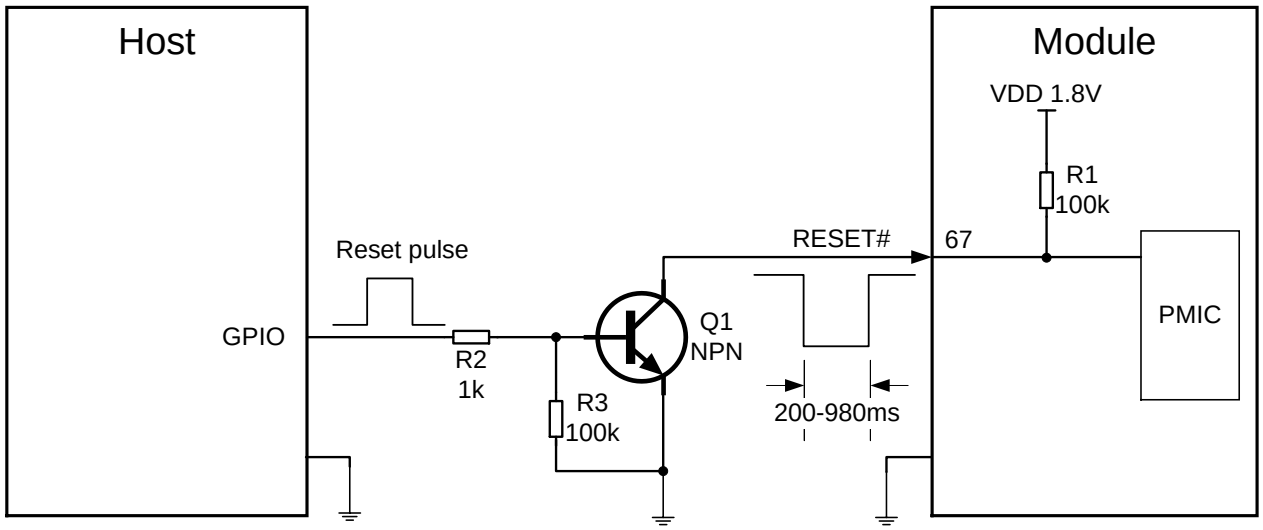
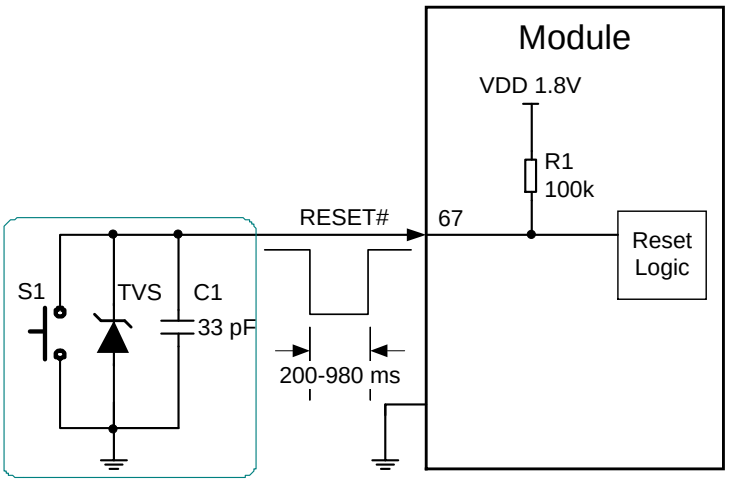


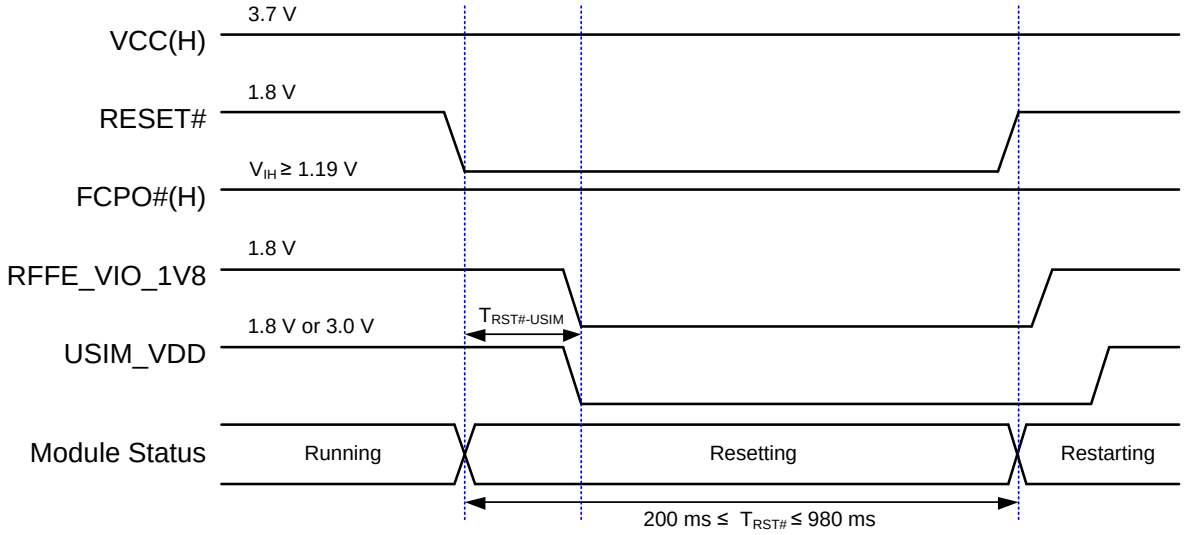
Figure 12: Reference Circuit of RESET# with NPN Driver Circuit



NOTE: The capacitor C1 is recommended to be less than 47 pF.

Figure 13: Reference Circuit of RESET# with Button

The reset timing is illustrated by the following figure.



NOTE: The host GPIO only needs to control RESET# to reset the module.

Figure 14: Reset Timing of the Module

Table 13: Reset Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{RST\#-USIM}$	200 ms			(U)SIM card turn-off time.
$T_{RST\#}$	200 ms	400 ms	980 ms	$T_{RST\#}$ ⩾ 980 ms will cause repeated reset.

4 Application Interfaces

The physical connections and signal levels of RM500Q-GL comply with PCI Express M.2 specification. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

- (U)SIM interfaces
- USB interface
- PCIe interface
- PCM interface
- Control and indication interfaces
- Cellular/WLAN COEX interface*
- Antenna tuner control interface*
- Configuration pins

4.1. (U)SIM Interfaces

The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported.

4.1.1. Pin Definition of (U)SIM

RM500Q-GL has two (U)SIM interfaces, and supports dual SIM single standby.

Table 14: Pin Definition of (U)SIM Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics
36	USIM1_VDD	PO	Power supply for (U)SIM1 card	1.8/3.0 V
34	USIM1_DATA	DIO, PU	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
32	USIM1_CLK	DO, PD	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
30	USIM1_RST	DO, PD	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V

66	USIM1_DET [1)]	DI, PU	(U)SIM1 card hot-plug detection.	1.8 V
48	USIM2_VDD	PO	Power supply for (U)SIM2 card	USIM2_VDD 1.8/3.0 V
42	USIM2_DATA	DIO, PU	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V
44	USIM2_CLK	DO, PD	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
46	USIM2_RST	DO, PD	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
40	USIM2_DET [1)]	DI, PU	(U)SIM2 card hot-plug detection.	1.8 V

NOTE

[1)] This pin is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.2. (U)SIM Hot-plug

The module supports (U)SIM card hot-plug via (U)SIM card hot-plug detection pins (USIM1_DET and USIM2_DET). (U)SIM card insertion is detected by high/low level. (U)SIM card hot-plug is disabled by default.

The following command enables (U)SIM card hot-plug function.

AT+QSIMDET (U)SIM Card Detection	
Test Command **AT+QSIMDET=?**	Response **+QSIMDET: (**list of supported **<enable>**s**),(**list of supported **<insert_level>**s**)** **OK**
Read Command **AT+QSIMDET?**	Response **+QSIMDET: <enable>,<insert_level>** **OK**
Write Command **AT+QSIMDET=<enable>,<insert_level>**	Response **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms

Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<enable>	Integer type. Enable or disable (U)SIM card detection. 0 Disable 1 Enable
<insert_level>	Integer type. The level of (U)SIM detection pin when a (U)SIM card is inserted. 0 Low level 1 High level

NOTES

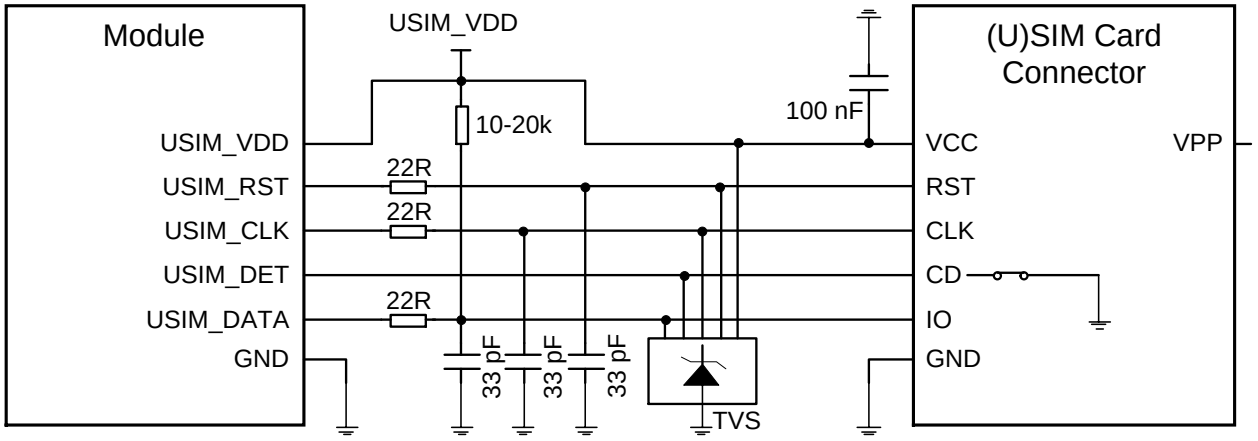
1. Hot-plug function is invalid if the configured value of **<insert_level>** is inconsistent with hardware design.
2. Hot-plug function setting takes effect after the module is restarted.
3. The underlined value is the default parameter value.
4. USIM_DET[1:2] is pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET pin is shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. After executing **AT+QSIMDET=1,1** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted, USIM_DET will change from low to high level; when the (U)SIM card is removed, USIM_DET will change from high to low level.

- When the (U)SIM is absent, CD is shorted to ground and USIM_DET is at low level.
- When the (U)SIM is present, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design for (U)SIM interface with a normally closed (U)SIM card connector.



NOTE:
All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

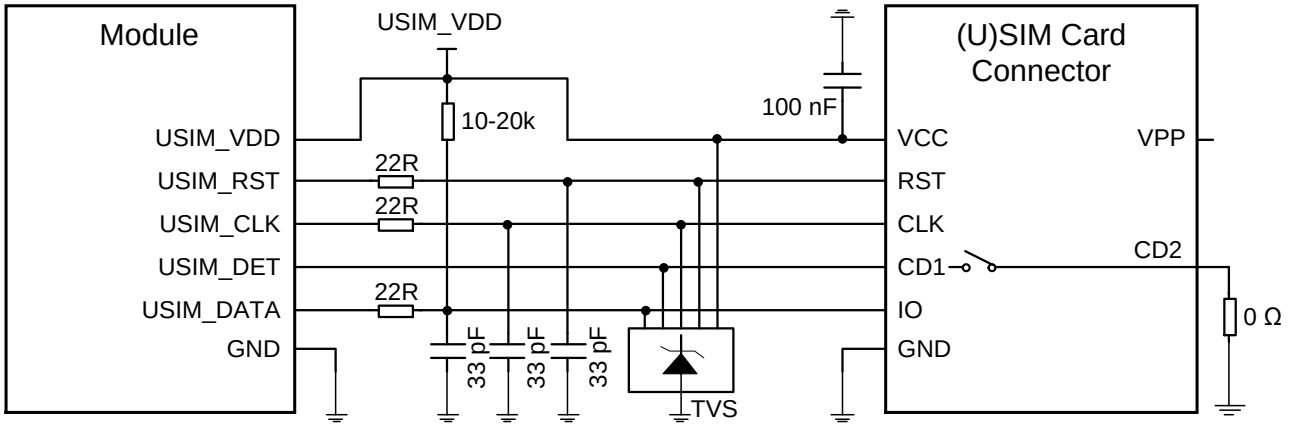
Figure 15: Reference Circuit for Normally Closed (U)SIM Card Connector

4.1.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. After executing **AT+QSIMDET=1,0** to enable the (U)SIM hot-plug: when a (U)SIM card is inserted, USIM_DET will change from high to low level; when the (U)SIM card is removed, USIM_DET will change from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high level.
- When the (U)SIM is present, CD1 is pull down to ground and USIM_DET is at low level.

The following figure shows a reference design for (U)SIM interface with a normally open (NO) (U)SIM card connector.

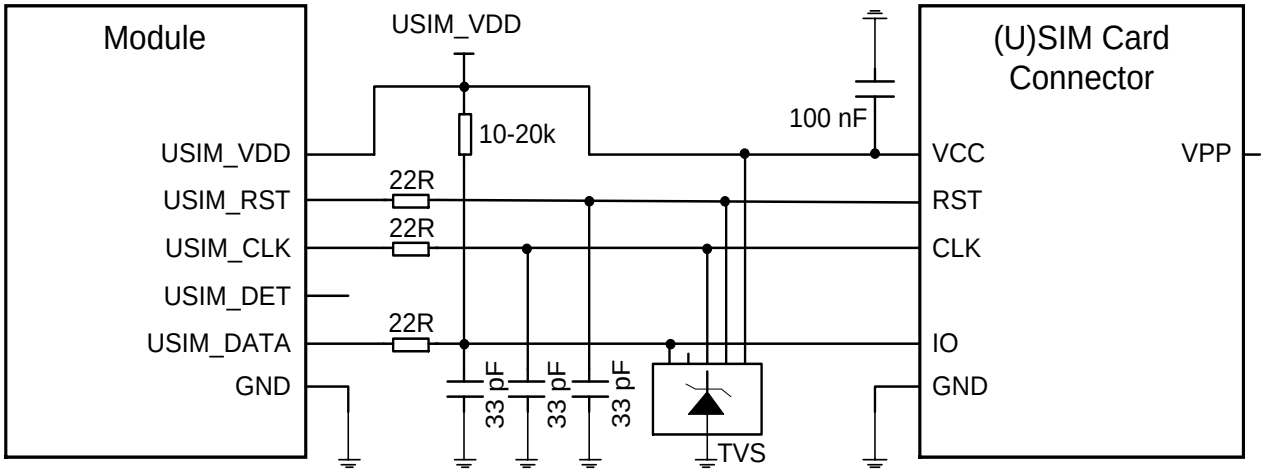


NOTE:
All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 16: Reference Circuit for Normally Open (U)SIM Card Connector

4.1.5. (U)SIM Card Connector Without Hot-plug

If (U)SIM card hot-plug is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated by the following figure.



NOTE:
All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 17: Reference Circuit for a 6-pin (U)SIM Card Connector

4.1.6. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS diode array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI such as spurious transmission, and to enhance ESD protection. The 33 pF capacitors are used to filter out RF interference.
- For USIM_DATA, a 10–20 kΩ pull-up resistor must be added near the (U)SIM card connector.

4.2. USB Interface

RM500Q-GL provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1/2.0 specifications and supports super speed (10 Gbps) on USB 3.1 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

Please note that only USB 2.0 can be used for firmware upgrade currently.

The following table shows the pin definition of USB interface.

Table 15: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB 2.0 differential data bus (+)	Requires differential impedance of 90 Ω
9	USB_DM	AIO	USB 2.0 differential data bus (-)	
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	

37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)

For more details about the USB 3.1 & 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit for USB 2.0/3.1 interface.

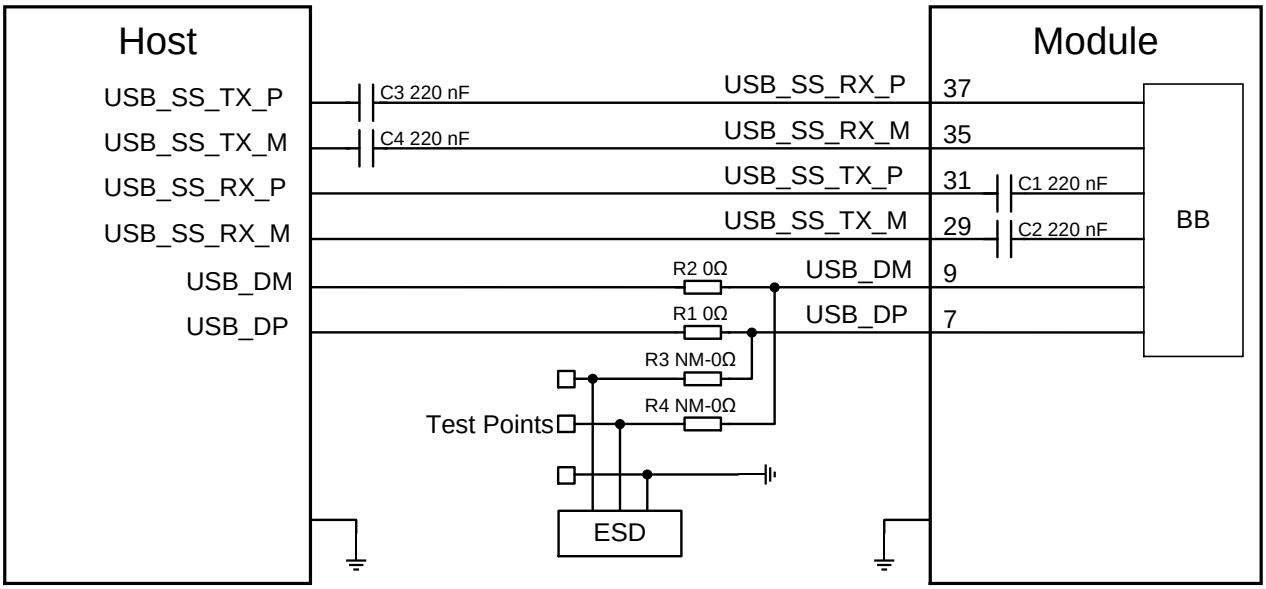


Figure 18: Reference Circuit for USB 3.1/2.0 Interface

AC coupling capacitors C3 and C4 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

You should follow the principles below when designing for the USB interface to meet USB 3.1 and 2.0 specifications:

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of differential trace of USB 2.0 and 3.1 is 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm, while the matching between Tx and Rx should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so you

should pay attention to the selection of the device. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.

- Keep the ESD protection devices as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM lines respectively.

4.3. PCIe Interface

RM500Q-GL provides one integrated PCIe (Peripheral Component Interconnect Express) interface.

- *PCI Express Base Specification Revision 3.0* compliant
- Data rate up to 8 Gbps per lane

4.3.1. PCIe Operating Mode

RM500Q-GL supports endpoint (EP) mode and root complex (RC) mode. In EP mode, the module is configured as a PCIe EP device. In RC mode, the module is configured as a PCIe root complex.

AT+QCFG="pcie/mode" is used to set PCIe RC/EP mode.

AT+QCFG="pcie/mode" Set PCIe RC/EP Mode	
Write Command **AT+QCFG="pcie/mode"[,<mode>]**	Response If the optional parameter is omitted, query the current setting: **+QCFG: "pcie/mode",<mode>** **OK** If the optional parameter is specified, set PCIe RC/EP mode: **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<mode>	Integer type. Set PCIe RC or EP mode.	
	0	PCIe EP mode.
	1	PCIe RC mode.

NOTES

1. The underlined value is the default parameter value.
2. For more details about the command, see ***document [4]***.

4.3.2. Pin Definition of PCIe

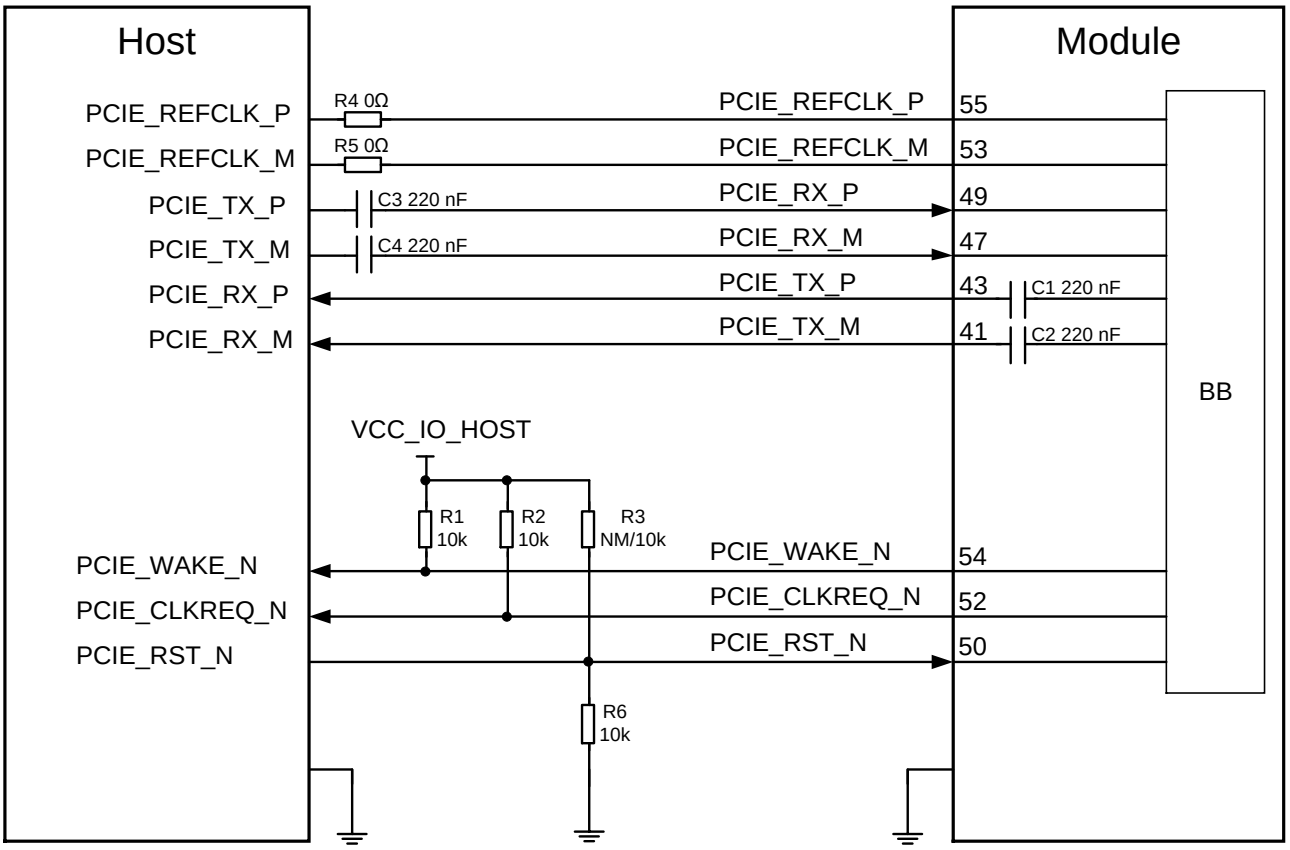
The following table shows the pin definition of PCIe interface.

Table 16: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz. Require differential impedance of 85 Ω
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 85 Ω
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 85 Ω
41	PCIE_TX_M	AO	PCIe transmit (-)	
50	PCIE_RST_N	DI, OD	PCIe reset. Active LOW	
52	PCIE_CLKREQ_N	DO, OD	PCIe clock request. Active LOW	
54	PCIE_WAKE_N	DO, OD	PCIe wake up Active LOW	

4.3.3. Reference design for PCIe

The following figure shows a reference circuit for the PCIe interface.



NOTE: The voltage level VCC_IO_HOST of these three signals depend on the host side due to open drain.

Figure 19: PCIe Interface Reference Circuit

To ensure the signal integrity of PCIe interface, AC coupling capacitors C3 and C4 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB.

The following principles of PCIe interface design should be complied with to meet the PCIe specification.

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, crystal and oscillator signals.
- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.

4.3.4. PCIe Timing

The following figure is PCIe power-up timing sequence for an adapter powered from system power rail in PCI Express M.2 specification.

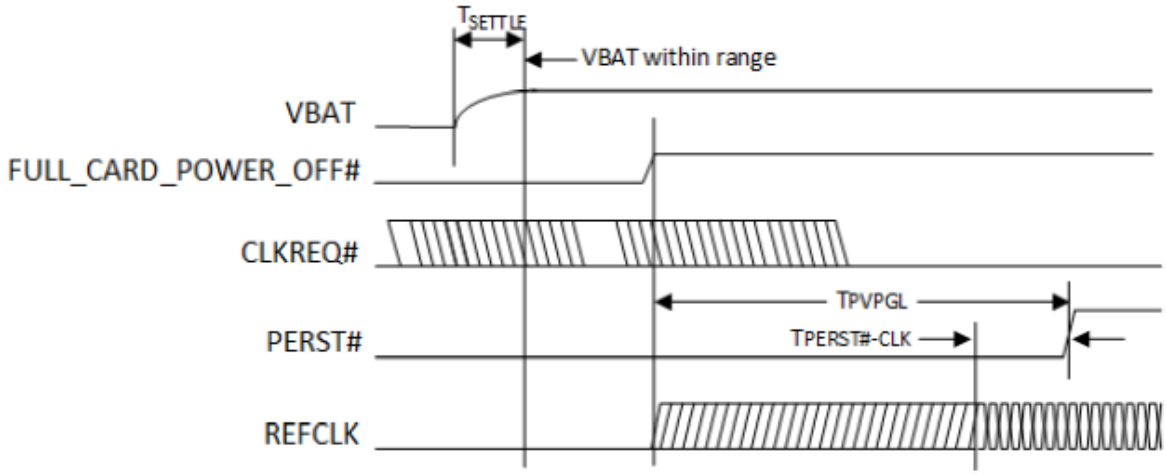


Figure 20: PCIe Power-on Timing Requirements of M.2 Specification

The following table is power-up timing variables in PCI Express M.2 specification.

Table 17: Power-up Timing of M.2 Specification

Symbol	Min.	Typ.	Max.	Comment
T_{PVPGL}	50 ms	-	-	Power valid to PERST# input inactive
$T_{PERST\#-CLK}$	100 µs	-	-	REFCLK stable before PERST# inactive

The following figure and table are PCIe turn-on timing and variables of the module.

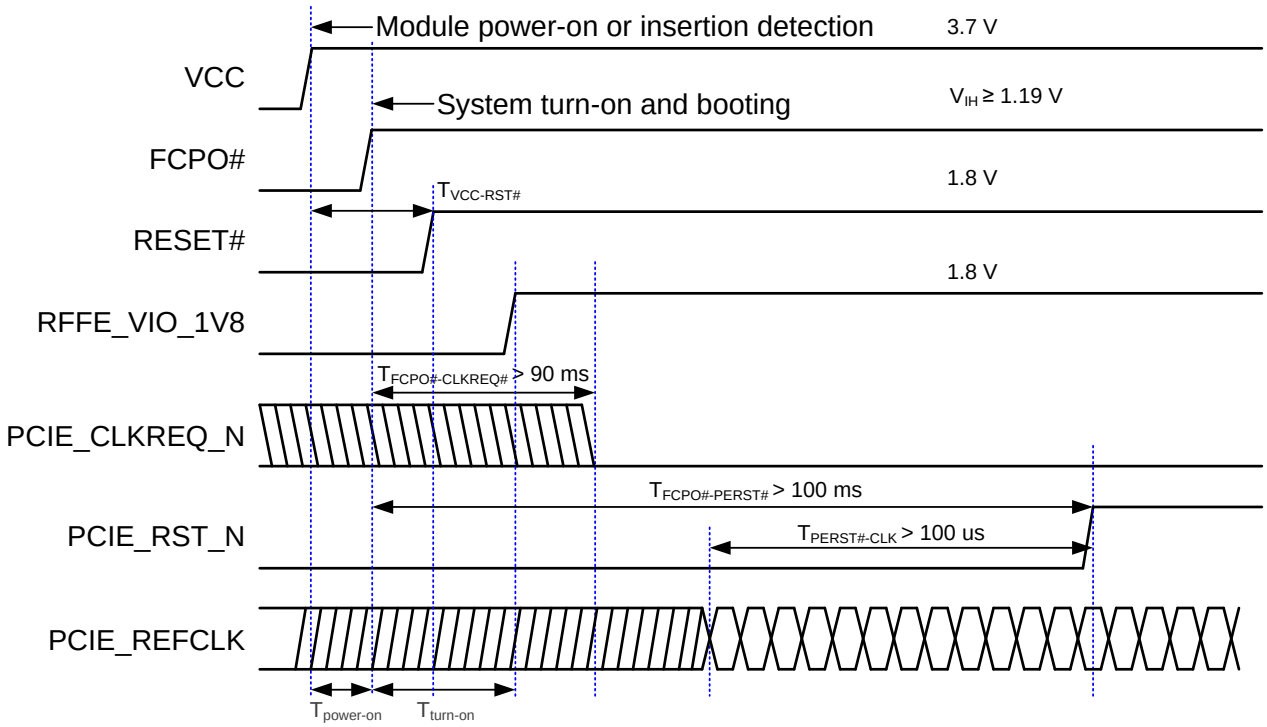


Figure 21: PCIe Power-on Timing of the Module

Table 18: PCIe Turn-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
$T_{power-on}$	0 ms	20 ms	-	Module power-on time depending on the host.
$T_{VCC-RST\#}$	-	33 ms	-	Time period between module power-on and RESET# being driven HIGH.
$T_{turn-on}$	68 ms	-	-	Module system turn on time.
$t_{FCPO\#-CLKREQ\#}$	90 ms	100 ms-	-	PCIe clock request.
$t_{FCPO\#-PERST}$	100 ms	-	-	PCIe reset.
$T_{PERST\#-CLK}$	100 µs	-	-	The time period during which REFCLK is stable before PERST# is inactive.

4.4. PCM Interface

RM500Q-GL supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave
- Auxiliary mode (long frame synchronization): the module works as master only

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

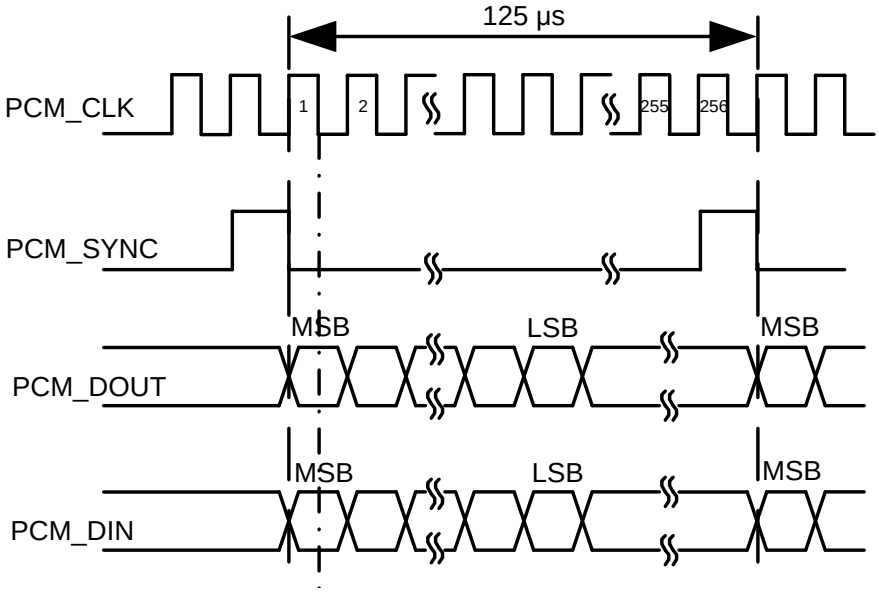


Figure 22: Primary Mode Timing

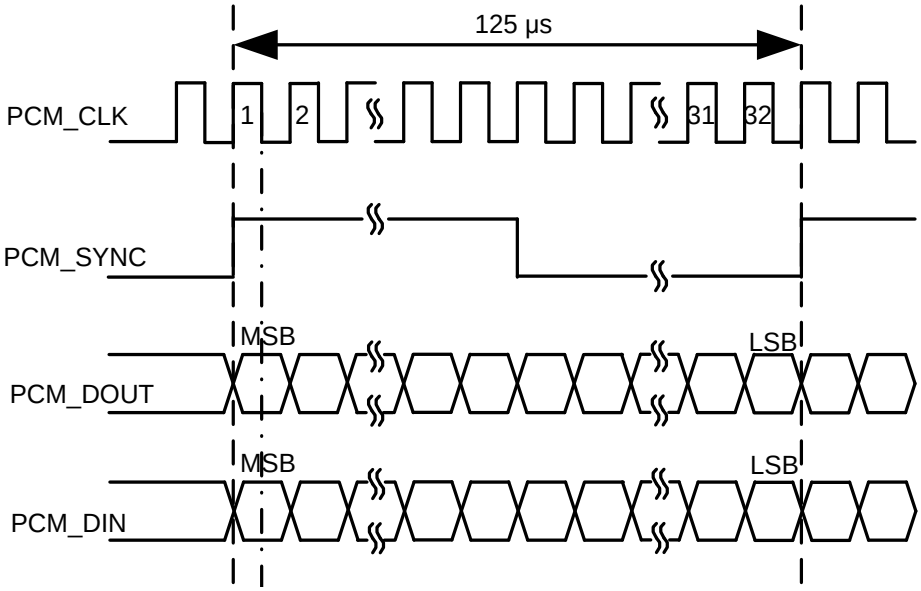


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface which can be applied to audio codec design.

Table 19: Pin Definition of PCM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
20	PCM_CLK	DIO, PD	PCM data bit clock	1.8 V
22	PCM_DIN	DI, PD	PCM data input	1.8 V
24	PCM_DOUT	DO, PD	PCM data output	1.8 V
28	PCM_SYNC	DIO, PD	PCM data frame sync	1.8 V

The clock and mode can be configured by AT command, and the default configuration is slave mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [4]*** for details about **AT+QDAI** command.

4.5. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

Table 20: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristic
8	W_DISABLE1#	DI, OD	Airplane mode control. Active LOW.	1.8/3.3 V
26	W_DISABLE2#	DI, OD	GNSS disable control. Active LOW.	1.8/3.3 V
10	WWAN_LED#	DO, OD	Indicate RF status of the module. Active LOW.	VCC
23	WAKE_ON_WAN#	DO, OD	Wake up the host. Active LOW.	1.8/3.3 V
25	DPR*	DI, PU	Dynamic power reduction. High voltage level by default.	1.8 V
38	SDX2AP_STATUS*	DO, PD	Status indication to AP	1.8 V
68	AP2SDX_STATUS*	DI, PD	Status indication from AP	1.8 V

4.5.1. W_DISABLE1#

RM500Q-GL provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. The W_DISABLE1# pin is pulled up by default. Driving it LOW will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through AT commands. The following table shows the AT command and corresponding RF function status of the module.

Table 21: RF Function Status

W_DISABLE1# Logic Level	AT Commands	RF Function Status
High	**AT+CFUN=1**	Enabled
High	**AT+CFUN=0** **AT+CFUN=4**	Disabled

Low	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled

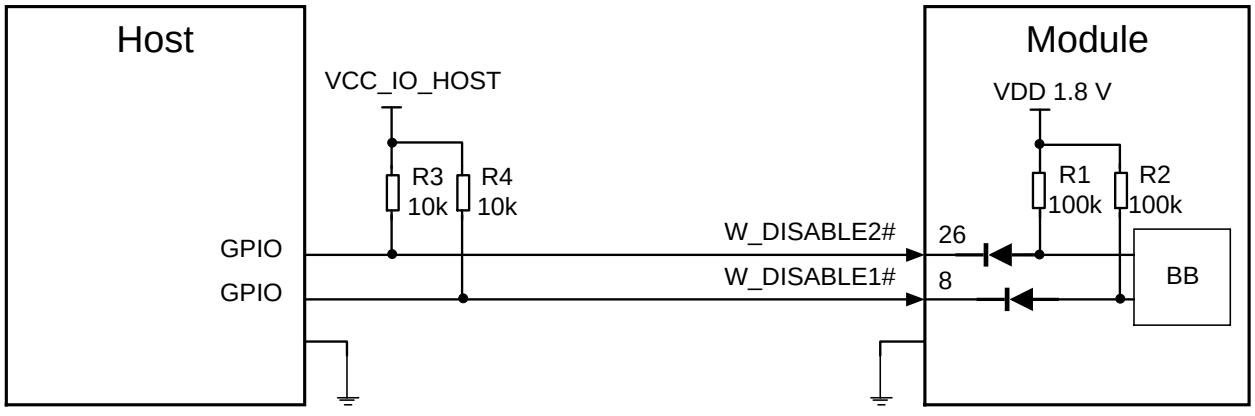
4.5.2. W_DISABLE2#

RM500Q-GL provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it low will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands controls the GNSS function.

Table 22: GNSS Function Status

W_DISABLE2# Logic Level	AT Commands	GNSS Function Status
High	**AT+QGPS=1**	Enabled
High	**AT+QGPSEND**	Disabled
Low	**AT+QGPS=1**	
Low	**AT+QGPSEND**	

A simple level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# pin which are pulled up to a 1.8 V voltage in the module, as shown in the following figure, so the control signals (GPIO) of the host device could be 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active LOW signals, and a reference circuit is presented below.



NOTE: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 24: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.5.3. WWAN_LED#

WWAN_LED# is used to indicate the RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated by the figure below. The LED is ON when the WWAN_LED# signal is at low level.

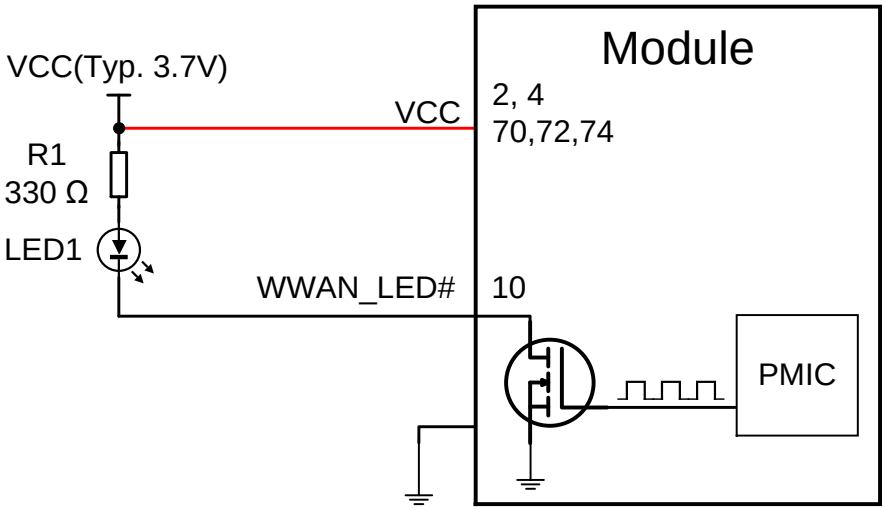


Figure 25: WWAN_LED# Reference Circuit

The following table shows the RF status indicated by WWAN_LED# signal.

Table 23: Network Status Indications of WWAN_LED#

WWAN_LED# Logic Level	Description
Low (LED on)	RF function is turned on
High (LED off)	RF function is turned off if any of the following occurs: ● The (U)SIM card is not powered. ● W_DISABLE1# is at low voltage level (airplane mode enabled). ● **AT+CFUN=4** (RF function disabled).

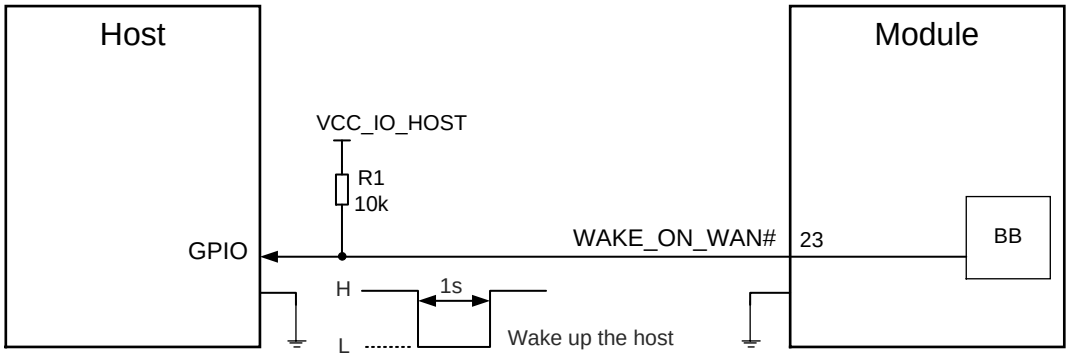
4.5.4. WAKE_ON_WAN#

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a one-second low level pulse signal will be outputted to wake up the host.

The module operation status indicated by WAKE_ON_WAN# is shown as below.

Table 24: State of WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Output a one-second pulse signal at low level	Call/SMS/Data is incoming (to wake up the host)
Always at high voltage level	Idle/Sleep



NOTE: The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 26: WAKE_ON_WAN# Signal Reference Circuit

4.5.5. DPR*

RM500Q-GL provides a DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from the proximity sensor of a host system to RM500Q-GL module to provide an input trigger, which will reduce the output power in radio transmission.

Table 25: Function of the DPR Signal

DPR Level	Function
High/Floating	NO max. transmitting power backoff
Low	Max. transmitting power backoff by **AT+QCFG="sarcfg"**

NOTE

See ***document [4]*** for more details about the command **AT+QCFG="sarcfg"**.

4.5.6. STATUS*

RM500Q-GL provides two status indication pins for communication with IPQ807x device. Pin 38 (SDX2AP_STATUS) outputs the status indication signal to IPQ807x device, and pin 68 (AP2SDX_STATUS) inputs the status indication signal from IPQ807x device. For more details, see ***document [5]***.

4.6. Cellular/WLAN COEX Interface*

RM500Q-GL provides a cellular/WLAN COEX interface, the following table shows the pin definition of this interface.

Table 26: Pin Definition of COEX Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
59	LAA_TX_EN*	DO	Notification from SDR to WLAN when LTE transmitting	1.8 V
60	WLAN_TX_EN*	DI	Notification from WLAN to SDR while transmitting	1.8 V
62	COEX_RXD*	DI, PD	LTE/WLAN coexistence receive	1.8 V
64	COEX_TXD*	DO, PD	LTE/WLAN coexistence transmit	1.8 V

4.7. Antenna Tuner Control Interface*

The module provides ANTCTL[1:2] and RFFE pins used for antenna tuner control, which should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

Table 27: Pin Definition of Antenna Tuner Control Interface

Pin No.	Pin Name	I/O	Description	DC Characteristic
56	RFFE_CLK [1)]	DO, PD	Used for external RFFE IC control	1.8 V
58	RFFE_DATA [1)]	DO, PD		1.8 V

65	RFFE_VIO_1V8 [1)]	PO	Power supply for RFFE	1.8 V Maximum output current: 50 mA
61	ANTCTL1*	DO, PD	Antenna Control	1.8 V
63	ANTCTL2*	DO, PD		1.8 V

NOTE

[1)] If this function is required, please contact Quectel for more details.

4.8. Configuration Pins

RM500Q-GL provides four configuration pins, which are defined as below.

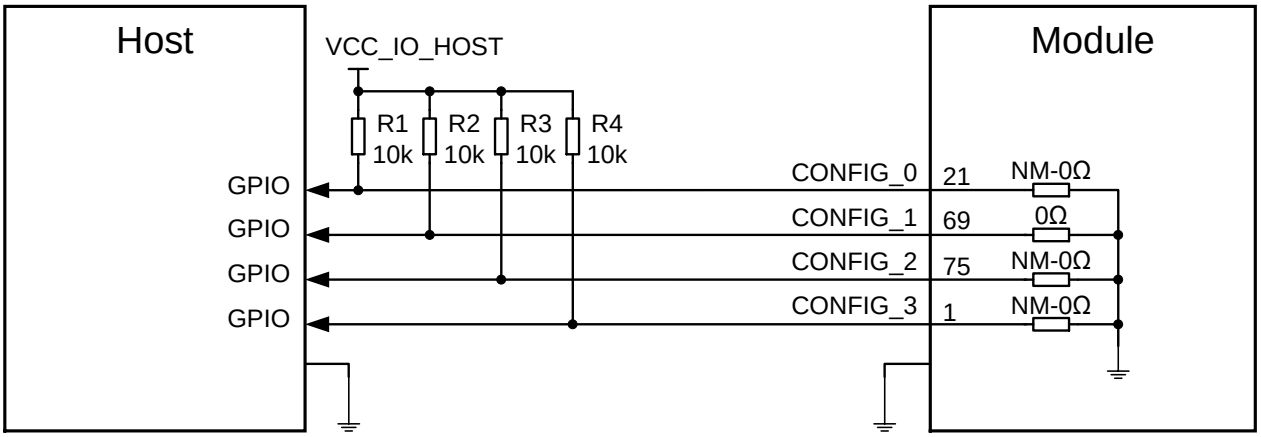
Table 28: Configuration Pins List of M.2 Specification

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	Quectel defined	2

Table 29: Configuration Pins of the Module

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit for these four pins.



NOTE: The voltage level of VCC_IO_HOST depends on the host side and could be 1.8 V or 3.3 V.

Figure 27: Recommended Circuit for Configuration Pins

5 RF Characteristic

This chapter mainly describes RF characteristics of RM500Q-GL. The module provides four antenna interfaces, ANT0, ANT1, ANT2_GNSSL1 and ANT3 and the impedance of them is 50 Ω.

5.1. Cellular Antenna Interfaces

5.1.1. Pin Definition

The pin definition of antenna interfaces is shown below.

Table 30: Pin Definition of RM500Q-GL Antenna Connectors

Pin Name	I/O	Description	Frequency
ANT0	AIO	Antenna 0 interface: **5G NR:** n41/n77/n78/n79 TRX1 [1)]; **LTE:** LMHB TRX & UHB PRX MIMO [2)] **WCDMA:** LMHB TRX	600–5000 MHz
ANT1	AIO	Antenna 1 interface: **5G NR:** n77/n78/n79 DRX0 & n41 TRX0; **LTE:** MHB PRX MIMO & UHB DRX [2)] & LAA PRX	1100–6000 MHz
ANT2_GNSSL1	AIO	Antenna 2 interface: **5G NR:** n77/n78/n79 DRX1 [1)] & n41 DRX0; **LTE:** MHB DRX MIMO & UHB DRX MIMO [2)] & LAA DRX; **GNSS:** L1	1400–6000 MHz
ANT3	AIO	Antenna 3 interface: **5G NR:** n77/n78/n79 TRX0 & n41 DRX1 [1)]; **LTE:** LMHB DRX & UHB TRX; **WCDMA:** LMHB DRX	600–5000 MHz

NOTES

1. [1)] NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.
2. [2)] LTE UHB frequency range: 3400–3800 MHz.

5.1.2. Pin Mapping

Table 31: RM500Q-GL Cellular Antenna Mapping

Antenna	5G NR			WCDMA/LTE	LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
	Refarmed	n41	n77/n78/n79					
ANT0	LMHB TRX	TRX1 [1)]	TRX1 [1)]	LTE LMHB TRX; LTE UHB PRX MIMO [2)]; WCDMA LMHB TRX;	617–960	1452–2690	3300–4200	4400–5000
ANT1	MHB PRX MIMO	TRX0	DRX0	LTE MHB PRX MIMO; LTE UHB DRX [2)]; LAA PRX;	-	1452–2690	3300–4200	4400–5000
ANT2_ GNSSL1	MHB DRX MIMO	DRX0	DRX1 [1)]	LTE MHB DRX MIMO; LTE UHB DRX MIMO [2)]; LAA DRX;	-	1452–2690	3300–4200	4400–5000
ANT3	LMHB DRX	DRX1 [1)]	TRX0	LTE LMHB DRX; LTE UHB TRX [2)]; WCDMA LMHB DRX;	617–960	1452–2690	3300–4200	4400–5000

NOTES

1. [1)] NR TRX1 = TX MIMO + PRX MIMO; NR DRX1 = DRX MIMO.
2. [2)] LTE UHB frequency range: 3400–3800 MHz.

5.1.3. Operating Frequency

Table 32: Module Operating Frequency

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	–	B1	n1
PCS (1900)	1850–1910	1930–1990	B2	–	B2	n2
DCS (1800)	1710–1785	1805–1880	B3	–	B3	n3
AWS	1710–1755	2110–2155	B4	–	B4	–
Cell (850)	824–849	869–894	B5	–	B5	n5
JCELL (800)	830–840	875–885	–	–	–	–
IMT-E (2600)	2500–2570	2620–2690	B7	–	–	n7

EGSM (950)	880–915	925–960	B8	–	B8	n8
J1700	1750–1785	1845–1880	–	–	–	–
700 lower A–C	699–716	729–746	B12	–	–	n12
700 upper C	777–787	746–756	B13	–	–	–
700 D	788–798	758–768	B14	–	–	–
B17	704–716	734–746	B17	–	–	–
B18	815–830	860–875	B18	–	–	–
B19	830–845	875–890	B19	–	B19	–
EU800	832–862	791–821	B20	–	–	n20
PCS + G	1850–1915	1930–1995	B25	–	–	–
B26	814–849	859–894	B26	–	–	–
700 APAC	703–748	758–803	B28	–	–	n28
FLO	–	717–728	B29	–	–	–
WCS	2305–2315	2350–2360	B30	–	–	–
L-band	–	1452–1496	B32	–	–	–
B34	2010–2025	2010–2025	–	B34	–	–
B38	2570–2620	2570–2620	–	B38	–	n38
B39	1880–1920	1880–1920	–	B39	–	–
B40	2300–2400	2300–2400	–	B40	–	n40
B41/B41-XGP	2496–2690	2496–2690	–	B41	–	n41
B42	3400–3600	3400–3600	–	B42	–	–
B43	3600–3800	3600–3800	–	B43	–	–
B46	5150–5925	5150–5925	–	B46	–	–
B48	3550–3700	3550–3700	–	B48	–	n48*
B66	1710–1780	2110–2200	B66	–	–	n66
B71	663–698	617–652	B71	–	–	n71
n77	3300–4200	3300–4200	–	–	–	n77
n78	3300–3800	3300–3800	–	–	–	n78

n79	4400–5000	4400–5000	–	–	–	n79

5.1.4. Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of the module.

Table 33: RM500Q-GL Conducted RF Receiving Sensitivity

Mode	Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA	WCDMA B1	-110	-110.8	-113	-106.7 dBm
	WCDMA B2	-110.5	-110.2	-113	-104.7 dBm
	WCDMA B3	-110.2	-110.6	-113	-103.7 dBm
	WCDMA B4	-110.6	-110.7	-113	-106.7 dBm
	WCDMA B5	-112.1	-113.4	-115	-104.7 dBm
	WCDMA B8	-112	-113	-115	-103.7 dBm
	WCDMA B19	-112.2	-113	-115	-104.7 dBm
LTE	LTE-FDD B1 (10 MHz)	-98.5	-99	-102	-96.3 dBm
	LTE-FDD B2 (10 MHz)	-98.5	-98.6	-101	-94.3 dBm
	LTE-FDD B3 (10 MHz)	-98	-98.6	-100.7	-93.3 dBm
	LTE-FDD B4 (10 MHz)	-98	-98.8	-101	-96.3 dBm
	LTE-FDD B5 (10 MHz)	-100.4	-101	-103.2	-94.3 dBm
	LTE-FDD B7 (10 MHz)	-98	-97.3	-100.3	-94.3 dBm
	LTE-FDD B8 (10 MHz)	-100	-101.1	-103	-93.3 dBm
	LTE-FDD B12 (10 MHz)	-100	-101	-103.5	-93.3 dBm
	LTE-FDD B13 (10 MHz)	-100.5	-101.5	-103.8	-93.3 dBm
	LTE-FDD B14 (10 MHz)	-100.5	-101	-103.8	-93.3 dBm
	LTE-FDD B17 (10 MHz)	-100.6	-101	-103	-93.3 dBm
	LTE-FDD B18 (10 MHz)	-100.4	-101	-103.5	-96.3 dBm

	LTE-FDD B19 (10 MHz)	-100.3	-100.8	-103.3	-96.3 dBm
	LTE-FDD B20 (10 MHz)	-101	-101.3	-104	-93.3 dBm
	LTE-FDD B25 (10 MHz)	-98	-98.6	-101.2	-92.8 dBm
	LTE-FDD B26 (10 MHz)	-100.6	-101.3	-103.4	-93.8 dBm
	LTE-FDD B28 (10 MHz)	-100.8	-101	-104	-94.8 dBm
	LTE-FDD B30 (10 MHz)	-97.5	-98.7	-101	-95.3 dBm
	LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	-95.3 dBm
	LTE-TDD B34 (10 MHz)	-98	-99.1	-101.3	-96.3 dBm
	LTE-TDD B38 (10 MHz)	-98.3	-97.3	-100.6	-96.3 dBm
	LTE-TDD B39 (10 MHz)	-97.3	-98.3	-100.8	-96.3 dBm
	LTE-TDD B40 (10 MHz)	-97.8	-97.9	-100.9	-96.3 dBm
	LTE-TDD B41 (10 MHz)	-98.4	-98	-101	-94.3 dBm
	LTE-TDD B42 (10 MHz)	-98.8	-96.2	-100.3	-95 dBm
	LTE-TDD B43 (10 MHz)	-99	96.2	-100.6	-95 dBm
	LTE-TDD B48 (10 MHz)	-96	-96	-98	-95 dBm
	LTE-TDD B66 (10 MHz)	-98.5	-99	-101.5	-95.8 dBm
	LTE-TDD B71 (10 MHz)	-101.5	-102	-104.7	-93.5 dBm
5G NR	5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-95	-96	-98	-94.0 dBm
	5G NR-FDD n2 (20 MHz) (SCS: 15 kHz)	-94	-93	-95	-92.0 dBm
	5G NR-FDD n3 (20 MHz) (SCS: 15 kHz)	-91	-91.5	-94	-91.0 dBm
	5G NR-FDD n5 (20 MHz) (SCS: 15 kHz)	-93	-94	-96	-91.0 dBm
	5G NR-FDD n7 (20 MHz) (SCS: 15 kHz)	-93.5	-93	-96	-92.0 dBm
	5G NR-FDD n8 (20 MHz) (SCS: 15 kHz)	-93	-94	-95.5	-90.0 dBm
	5G NR-FDD n12 (15 MHz) (SCS: 15 kHz)	-90.5	-95.5	TBD	-94.0 dBm

	5G NR-FDD n20 (20 MHz) (SCS: 15 kHz)	-92.5	-94.5	-95.5	-89.8 dBm
	5G NR-FDD n25 (20 MHz) (SCS: 15 kHz)	-91	-91	-94	-90.5 dBm
	5G NR-FDD n28 (20 MHz) (SCS: 15 kHz)	-97	-98	-99.5	-90.8 dBm
	5G NR-TDD n38 (20 MHz) (SCS: 30 kHz)	-94	-93.5	-97	-90.6 dBm
	5G NR-TDD n40 (20 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-94.0 dBm
	5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-83.5	-83.5	-87	-84.0 dBm
	5G NR-FDD n48* (20 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	--92.9 dBm
	5G NR-FDD n66 (20 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.5 dBm
	5G NR-FDD n71 (20 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-85.3 dBm
	5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-85	-84	-90	-87.8 dBm
	5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-84.5	-87	-90	-87.8 dBm
	5G NR-TDD n79 (100 MHz) (SCS: 30 kHz)	-84.5	-87	TBD	-87.8 dBm

NOTE

[1] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which improves Rx performance.

5.1.5. Output Power

The following table shows the RF output power of the module.

Table 34: RF Output Power

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	24 dBm +1/-3 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm

	LTE HPUE bands (B38/B40/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm (BW: 5–20 MHz) [1)]
	5G NR HPUE bands (n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm (BW: 5–20 MHz) [1)]

NOTE

[1)] For 5G NR TDD bands, the normative reference for this requirement is *3GPP TS 38.101-1 clause 6.3.1*.

5.2. GNSS Antenna Interface

5.2.1. General Description

The module includes a fully integrated global navigation satellite system solution that supports Qualcomm Gen9C Lite (GPS, GLONASS, BeiDou/COMPASS, and Galileo).

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine is switched off by default. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document [6]***.

5.2.2. GNSS Frequency

The following table shows the frequency specification of GNSS antenna connector.

Table 35: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42 ±1.023 (L1)	MHz
Galileo	1575.42 ±2.046 (E1)	MHz
QZSS	1575.42 (L1)	MHz
GLONASS	1597.5–1605.8	MHz
BeiDou/COMPASS	1561.098 ±2.046	MHz

NOTES

1. Keep the characteristic impedance for the trace of GNSS antenna (ANT2_GNSSL1) to 50 Ω.
2. Place the π-type matching components as close to the antenna as possible.
3. Keep the digital circuits, such as that of (U)SIM card, USB interface, camera module, display connector and SD card, away from the antenna traces.
4. Keep 75 dB isolation between each antenna trace.
5. Keep 15 dB isolation between each antenna to improve the receiving sensitivity. and 20 dB isolation between 5G NR UL MIMO TRX0 and TRX1 antennas.

5.2.3. GNSS Performance

The following table shows GNSS performance of RM500Q-GL series module.

Table 36: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-147	dBm
	Reacquisition	Autonomous	-159	dBm
	Tracking	Autonomous	-159	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	33.7	s
		XTRA enabled	18.9	s
	Warm start @ open sky	Autonomous	33.4	s
		XTRA enabled	1.5	s
	Hot start @ open sky	Autonomous	1.1	s
		XTRA enabled	1.1	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	1.02	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain locked (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain

locked within 3 minutes after the loss of lock.

3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.3. Antenna Connectors

5.3.1. Antenna Connector Location

RM500Q-GL has four antenna connectors: ANT0, ANT1, ANT2_GNSSL1 and ANT3, which are shown below.

Figure 28: Antenna Connectors on the Module

5.3.2. Antenna Connector Size

RM500Q-GL is mounted with standard 2 mm × 2 mm receptacle antenna connectors for convenient antenna connection. The antenna connector's PN is IPEX 20579-001E, and the connector dimensions are illustrated as below:

The connector dimensions are illustrated by the figure below:

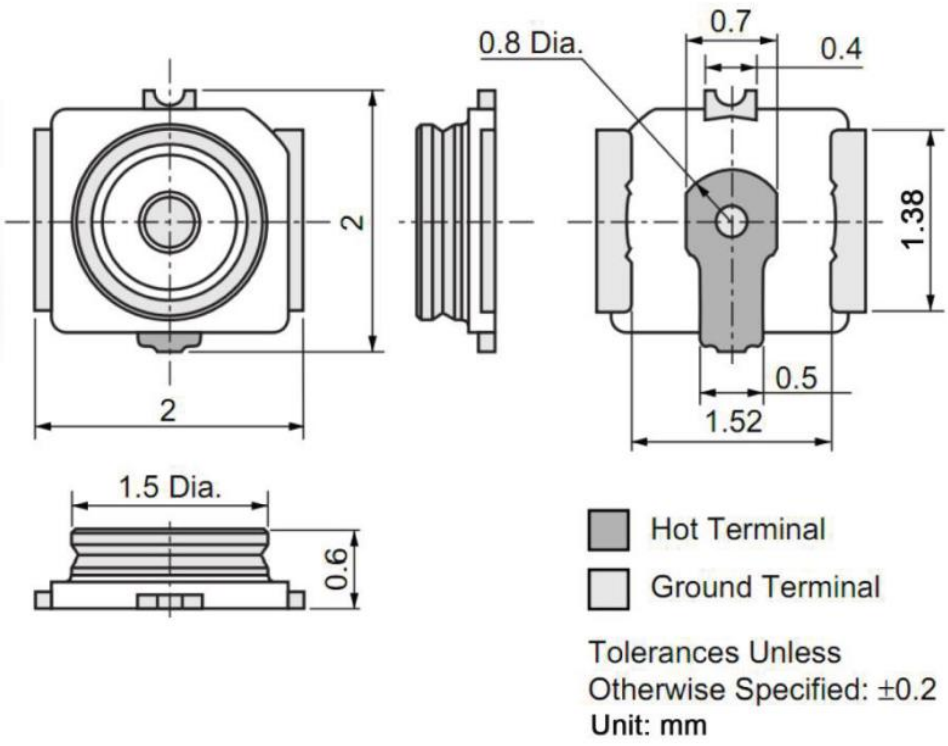


Figure 29: RM500Q-GL RF Connector Dimensions (Unit: mm)

Table 37: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

5.3.3. Antenna Connector Installation

The receptacle RF connector used in conjunction with RM500Q-GL will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø 0.81 mm coaxial cables.

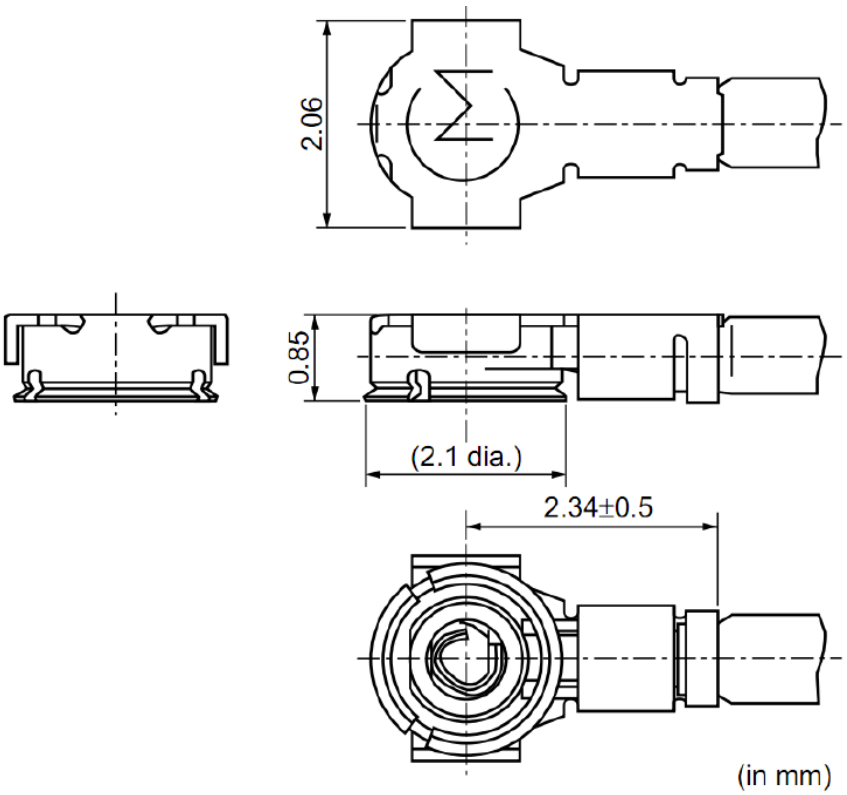


Figure 30: Specifications of Mating Plugs Using Ø 0.81 mm Coaxial Cables

The following figure illustrates the connection between the receptacle RF connector on RM500Q-GL and the mating plug using a Ø 0.81 mm coaxial cable.

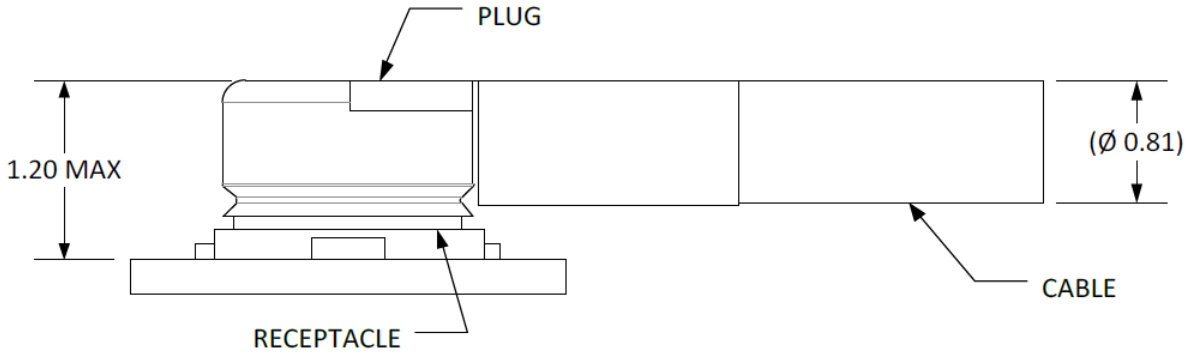


Figure 31: Connection between RF Connector and Mating Plug Using Ø 0.81 mm Coaxial Cable

The following figure illustrates the connection between the receptacle RF connector on RM500Q-GL and the mating plug using a Ø 1.13 mm coaxial cable.

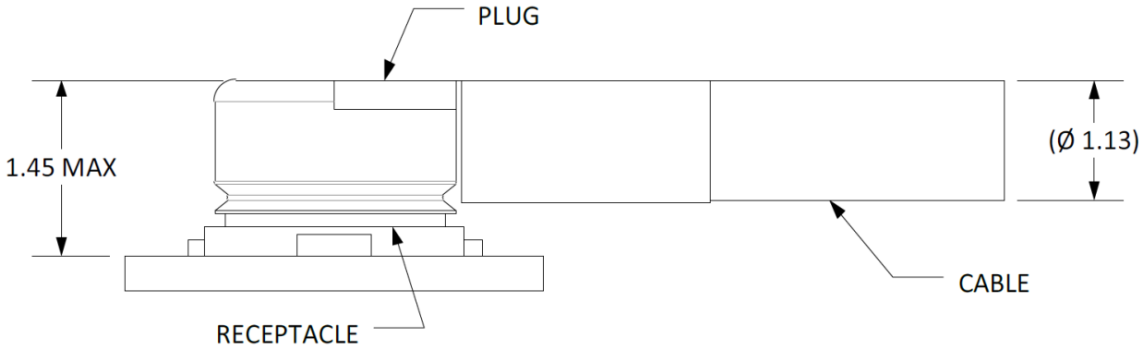


Figure 32: Connection between RF Connector and Mating Plug Using Ø 1.13 mm Coaxial Cable

5.3.4. Recommended RF Connector for Installation

5.3.4.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

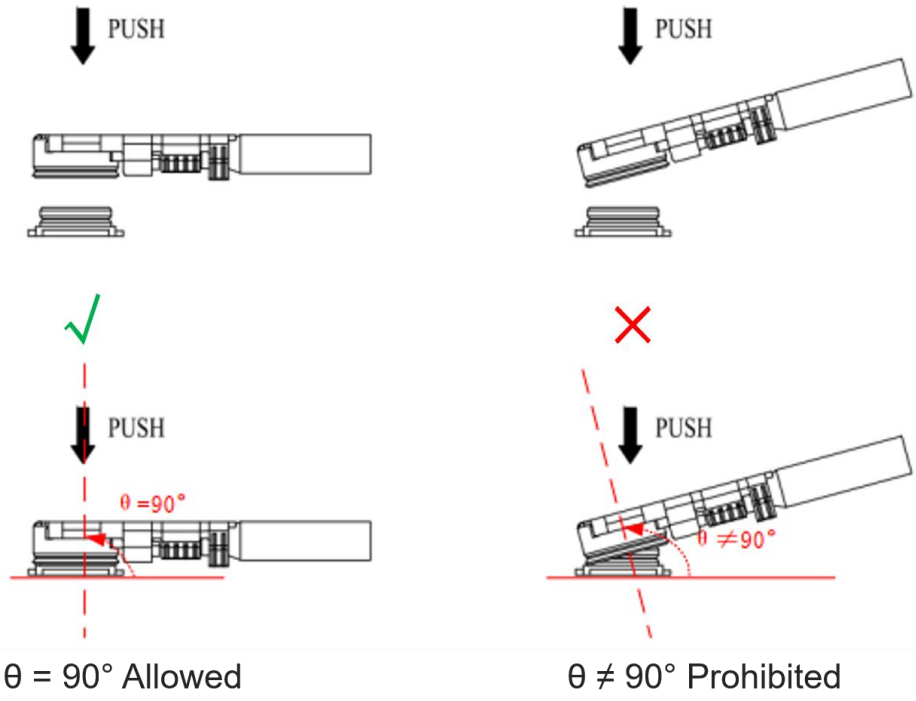


Figure 33：Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

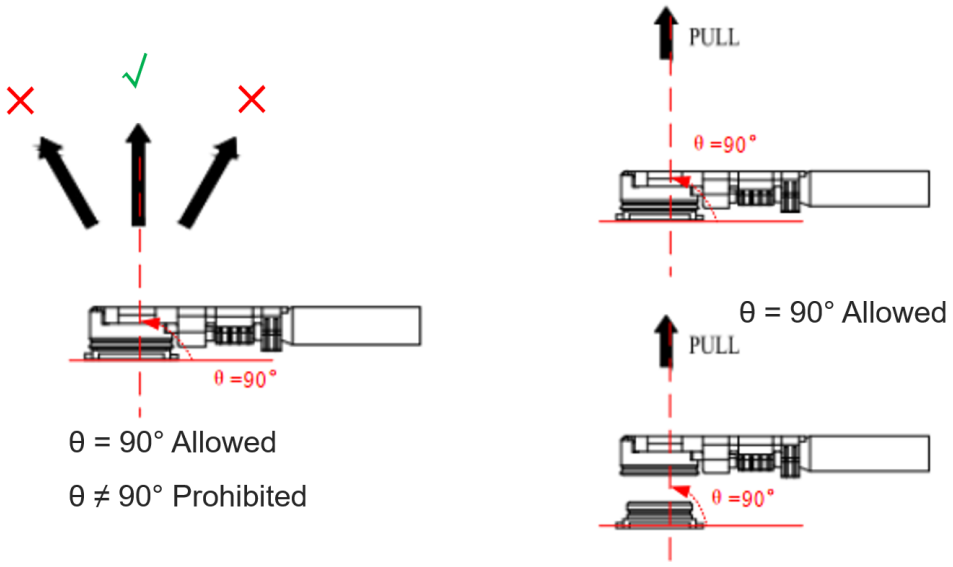


Figure 34：Pull out a Coaxial Cable Plug

5.3.4.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

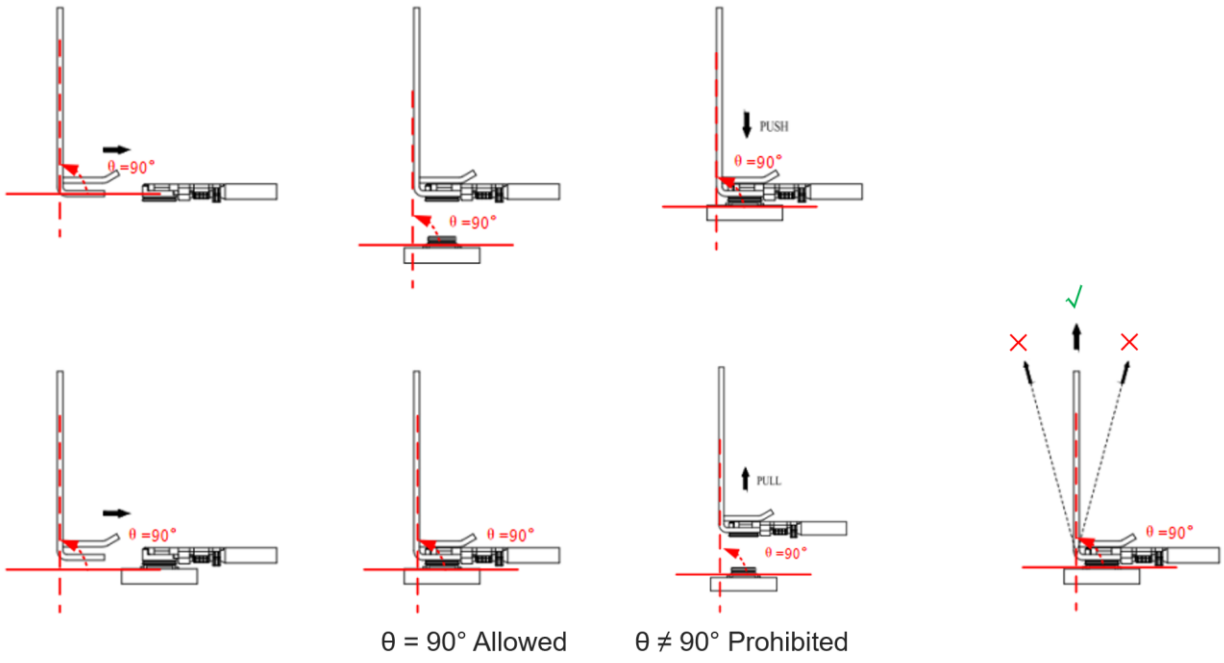


Figure 35：Install the Coaxial Cable Plug with Jig

5.3.5. Recommended Manufacturers of RF Connector and Cable

RF connecters and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

5.4. Antenna Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antenna.

Table 38: Antenna Requirements

Type	Requirements
GNSS	● Frequency range: 1559–1606 MHz ● Polarization: RHCP or linear ● VSWR: < 2 (typ.) ● Passive antenna gain: > 0 dBi
WCDMA/LTE/5G NR	● VSWR: ≤ 3 ● Efficiency: > 30 % ● Input Impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** WCDMA B5/B8/B19 LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28/B29/B71 5G NR n5/n8/n12/n20/n28/n71 **< 1.5 dB:** WCDMA B1/B2/B3/B4 LTE B1/B2/B3/B4/B25/B32/B34/B39/B66 5G NR n1/n2/n3/n25/n66 **< 2 dB:** LTE B7/B30/B38/B40/B41/B42/B43/B46/B48 5G NR n7/n38/n40/n41/n48*/n77/n78/n79

6 Electrical Characteristics and Reliability

6.1. Power Supply Requirements

The typical input voltage of RM500Q-GL is 3.7 V. The following table shows the power supply requirements of RM500Q-GL.

Table 39: Power Supply Requirement

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple		-	30	100	mV
Voltage Drop		-	-	165	mV

6.2. Current Consumption

Table 40: RM500Q-GL Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	71.8	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	4.615	mA
	WCDMA PF = 64 (USB disconnected)	6.11	mA
	LTE-FDD PF = 64 (USB disconnected)	6.98	mA

	LTE-TDD PF = 64 (USB disconnected)	7.04	mA
Idle state	WCDMA PF = 64 (USB disconnected)	40.97	mA
	WCDMA PF = 64 (USB connected)	66.96	mA
	LTE-FDD PF = 64 (USB disconnected)	42.56	mA
	LTE-FDD PF = 64 (USB connected)	68.67	mA
	LTE-TDD PF = 64 (USB disconnected)	42.67	mA
	LTE-TDD PF = 64 (USB connected)	68.56	mA
WCDMA (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 23 dBm	480	mA
	WCDMA B1 HSUPA CH10700 @ 23 dBm	460	mA
	WCDMA B2 HSDPA CH9800 @ 23 dBm	490	mA
	WCDMA B2 HSUPA CH9800 @ 23 dBm	460	mA
	WCDMA B3 HSDPA CH1338 @ 23 dBm	510	mA
	WCDMA B3 HSUPA CH1338 @ 23 dBm	500	mA
	WCDMA B4 HSDPA CH1638 @ 23 dBm	440	mA
	WCDMA B4 HSUPA CH1638 @ 23 dBm	440	mA
	WCDMA B5 HSDPA CH4407 @ 23 dBm	380	mA
	WCDMA B5 HSUPA CH4407 @ 23 dBm	370	mA
	WCDMA B8 HSDPA CH3012 @ 23 dBm	420	mA
	WCDMA B8 HSUPA CH3012 @ 23 dBm	400	mA
	WCDMA B19 HSDPA CH738 @ 23 dBm	390	mA
	WCDMA B19 HSUPA CH738 @ 23 dBm	390	mA
	LTE-FDD B1 CH18300 @ 23 dBm	680	mA
	LTE-FDD B2 CH18900 @ 23 dBm	650	mA
LTE (GNSS OFF)	LTE-FDD B3 CH19575 @ 23 dBm	740	mA
	LTE-FDD B4 CH20175 @ 23 dBm	640	mA

	LTE-FDD B5 CH20525 @ 23 dBm	440	mA
	LTE-FDD B7 CH21100 @ 23 dBm	720	mA
	LTE-FDD B8 CH21625 @ 23 dBm	450	mA
	LTE-FDD B12 CH23095 @ 23 dBm	440	mA
	LTE-FDD B13 CH23230 @ 23 dBm	480	mA
	LTE-FDD B14 CH23330 @ 23 dBm	440	mA
	LTE-FDD B17 CH5790 @ 23 dBm	470	mA
	LTE-FDD B18 CH23925 @ 23 dBm	470	mA
	LTE-FDD B19 CH24075 @ 23 dBm	450	mA
	LTE-FDD B20 CH24300 @ 23 dBm	440	mA
	LTE-FDD B25 CH26365 @ 23 dBm	660	mA
	LTE-FDD B26 CH26865 @ 23 dBm	450	mA
	LTE-FDD B28 CH27435 @ 23 dBm	510	mA
	LTE-FDD B30 CH27710 @ 23 dBm	780	mA
	LTE-TDD B34 CH36275 @ 23 dBm	290	mA
	LTE-TDD B38 CH38000 @ 23 dBm	430	mA
	LTE-TDD B39 CH38450 @ 23 dBm	350	mA
	LTE-TDD B40 CH39150 @ 23 dBm	340	mA
	LTE-TDD B41 CH40620 @ 23 dBm	400	mA
	LTE-TDD B42 CH42590 @ 23 dBm	400	mA
	LTE-TDD B43 CH44590 @ 23 dBm	410	mA
	LTE-TDD B48 CH55990 @ 23 dBm	450	mA
	LTE-FDD B66 CH132422 @ 23 dBm	700	mA
	LTE-FDD B71 CH132297 @ 23 dBm	460	mA
	5G NR-TDD n41 CH501204 @ 23 dBm	TBD	mA

	5G NR-TDD n41 CH518598 @ 23 dBm	TBD	mA
5G NR (GNSS OFF)	5G NR-TDD n41 CH535998 @ 23 dBm	TBD	mA
	5G NR-TDD n77 CH620668 @ 23 dBm	TBD	mA
	5G NR-TDD n77 CH650000 @ 23 dBm	TBD	mA
	5G NR-TDD n77 CH679332 @ 23 dBm	TBD	mA
	5G NR-TDD n78 CH620668 @ 23 dBm	TBD	mA
	5G NR-TDD n78 CH636666 @ 23 dBm	TBD	mA
	5G NR-TDD n78 CH652666 @ 23 dBm	TBD	mA
	5G NR-TDD n79 CH695090 @ 23 dBm	TBD	mA
	5G NR-TDD n79 CH713522 @ 23 dBm	TBD	mA
	5G NR-TDD n79 CH731976 @ 23 dBm	TBD	mA
	5G NR-FDD n1 CH423000 @ 23 dBm	TBD	mA
	5G NR-FDD n1 CH428000 @ 23 dBm	490	mA
	5G NR-FDD n1 CH433000 @ 23 dBm	TBD	mA
	5G NR-FDD n2 CH387000 @ 23 dBm	TBD	mA
	5G NR-FDD n2 CH392000 @ 23 dBm	450	mA
	5G NR-FDD n2 CH397000 @ 23 dBm	TBD	mA
	5G NR-FDD n3 CH362000 @ 23 dBm	TBD	mA
	5G NR-FDD n3 CH368500 @ 23 dBm	480	mA
	5G NR-FDD n3 CH375000 @ 23 dBm	TBD	mA
	5G NR-FDD n5 CH174800 @ 23 dBm	TBD	mA
	5G NR-FDD n5 CH176300 @ 23 dBm	370	mA
	5G NR-FDD n5 CH177800 @ 23 dBm	TBD	mA
	5G NR-FDD n7 CH525000 @ 23 dBm	TBD	mA
	5G NR-FDD n7 CH531000 @ 23 dBm	500	mA

	5G NR-FDD n7 CH537000 @ 23 dBm	TBD	mA
	5G NR-FDD n8 CH186000 @ 23 dBm	TBD	mA
	5G NR-FDD n8 CH188500 @ 23 dBm	370	mA
	5G NR-FDD n8 CH191000 @ 23 dBm	TBD	mA
	5G NR-FDD n12 CH146800 @ 23 dBm	TBD	mA
	5G NR-FDD n12 CH147500 @ 23 dBm	350	mA
	5G NR-FDD n12 CH148200 @ 23 dBm	TBD	mA
	5G NR-FDD n20 CH159200 @ 23 dBm	TBD	mA
	5G NR-FDD n20 CH161200 @ 23 dBm	370	mA
	5G NR-FDD n20 CH163200 @ 23 dBm	TBD	mA
	5G NR-FDD n28 CH152600 @ 23 dBm	TBD	mA
	5G NR-FDD n28 CH156100 @ 23 dBm	350	mA
	5G NR-FDD n28 CH159600 @ 23 dBm	TBD	mA
	5G NR-TDD n38 CH515000 @ 23 dBm	TBD	mA
	5G NR-TDD n38 CH519000 @ 23 dBm	TBD	mA
	5G NR-TDD n38 CH523000 @ 23 dBm	TBD	mA
	5G NR-TDD n40 CH461000 @ 23 dBm	TBD	mA
	5G NR-TDD n40 CH470000 @ 23 dBm	TBD	mA
	5G NR-TDD n40 CH479000 @ 23 dBm	TBD	mA
	5G NR-FDD n66 CH423000 @ 23 dBm	TBD	mA
	5G NR-FDD n66 CH429000 @ 23 dBm	450	mA
	5G NR-FDD n66 CH435000 @ 23 dBm	TBD	mA
	5G NR-FDD n71 CH124400 @ 23 dBm	TBD	mA
	5G NR-FDD n71 CH126900 @ 23 dBm	360	mA
	5G NR-FDD n71 CH129400 @ 23 dBm	TBD	mA

	WCDMA B1 CH10700 @ 23 dBm	560	mA
	WCDMA B2 CH9800 @ 23 dBm	570	mA
WCDMA voice call	WCDMA B3 CH1338 @ 23 dBm	600	mA
	WCDMA B4 CH1638 @ 23 dBm	570	mA
	WCDMA B5 CH4408 @ 23 dBm	410	mA
	WCDMA B6 CH4175 @ 23 dBm	TBD	mA
	WCDMA B8 CH3012 @ 23 dBm	420	mA
	WCDMA B19 CH338 @ 23 dBm	440	mA

6.3. Digital I/O Characteristic

Table 41: Logic Levels of Digital I/O (1.8 V)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.65	2.1	V
V_{IL}	Input low voltage	-0.3	0.54	V
V_{OH}	Output high voltage	1.3	1.8	V
V_{OL}	Output low voltage	0	0.4	V

Table 42: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

Table 43: (U)SIM 3.0V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

6.4. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

Table 44: Electrostatic Discharge Characteristics (Temperature: 25 ºC, Humidity: 40 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.5. Thermal Dissipation

RM500Q-GL is designed to work in an extended temperature range. To achieve a maximum performance while working under extended temperatures or extreme conditions (such as with maximum power or data rate) for a long time, it is strongly recommended to add a thermal pad or other thermally conductive compounds between the module and the main PCB for thermal dissipation.

The thermal dissipation area on the bottom (i.e. the area for adding thermal pad) is shown below, and thermal paste are also added on the BB, MCP, PMU, WTR, PA-1, PA-2 chips inside the module. The dimensions are measured in mm.

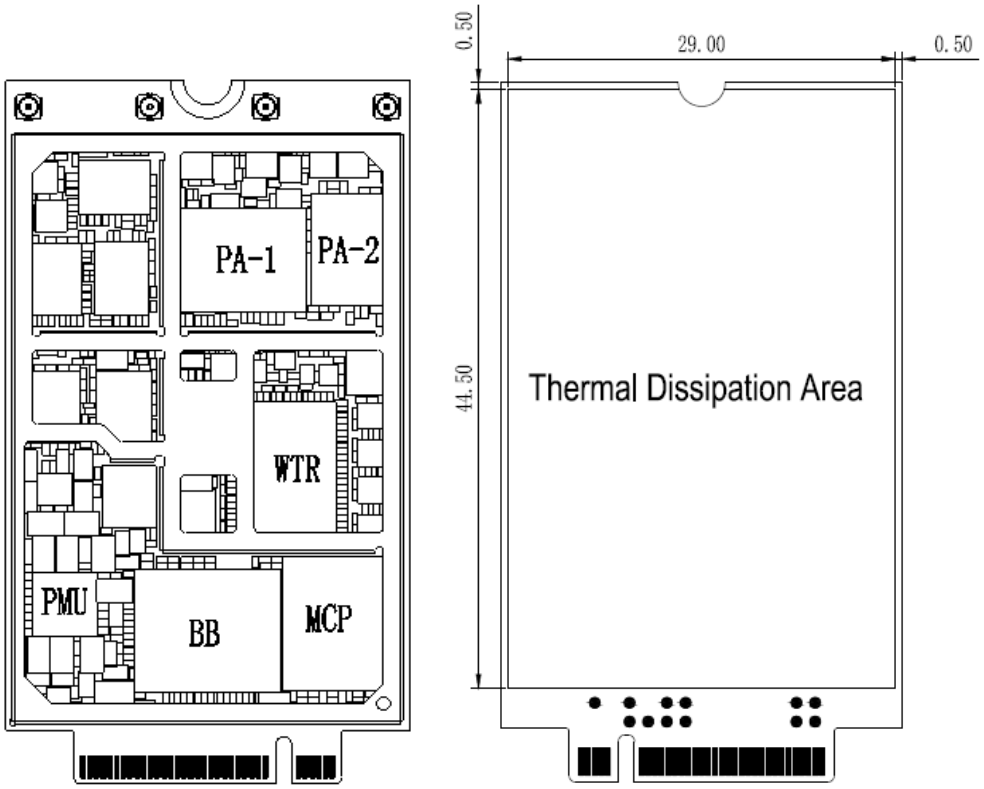


Figure 36: Thermal Dissipation Area Inside and on Bottom Side of the Module (Unit: mm)

There are other measures to enhance heat dissipation performance:

- Add as many ground vias as possible on the PCB.
- Maximize airflow over/around the module.
- Place the module away from other heating sources.
- Module mounting holes must be used to attach (ground) the device to the main PCB ground.
- It is NOT recommended to apply solder mask on the main PCB where the module's thermal dissipation area is located.
- Select appropriate material, thickness and surface for the outer housing of the application device that integrates the module (i.e., the mechanical enclosure) to enhance thermal dissipation ability. You may also need active cooling to dissipate heat of the module.
- If possible, add a heatsink on the top of the module. A thermal pad should be used between the heatsink and the module, and the heatsink should be designed with as many fins as possible to increase heat dissipation area.

NOTE

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

6.6. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 45: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
VCC	-0.3		4.7	V
Voltage at Digital Pins	-0.3		2.3	V

6.7. Operating and Storage Temperatures

Table 46: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-30	+25	+70	ºC
Extended Temperature Range [2)]	-40	-	+85	ºC
Storage temperature Range	-40	-	+90	ºC

NOTES

1. [1)] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module meets 3GPP specifications.
2. [2)] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of RM500Q-GL module. All dimensions are measured in mm, and the tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

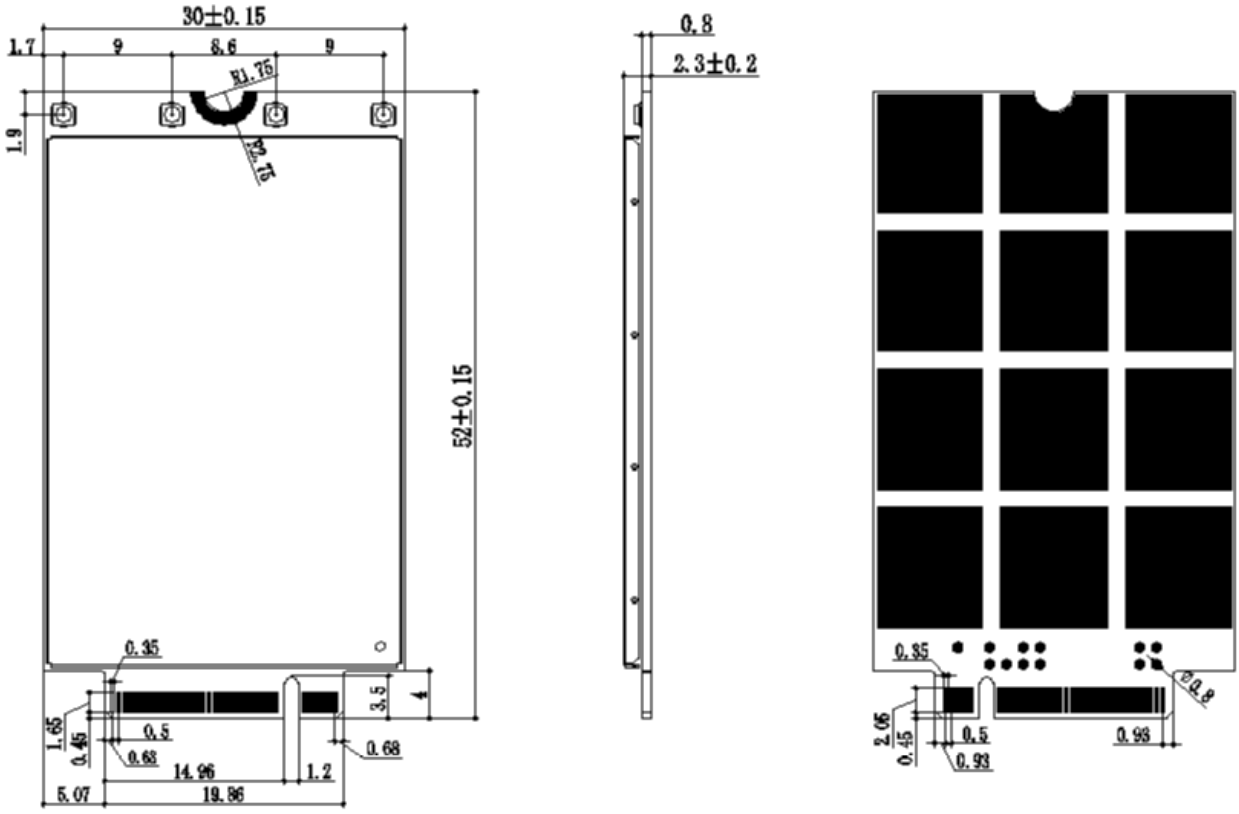


Figure 37: Mechanical Dimensions of RM500Q-GL (Unit: mm)

7.2. Top and Bottom Views of the Module

Figure 38: Top and Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7.3. M.2 Connector

RM500Q-GL adopts a standard PCI Express M.2 connector which compiles with the directives and standards listed in *PCI Express M.2 Specification Revision 3.0, Version 1.2.*

7.4. Packaging

RM500Q-GL modules are packaged in trays. The following figure shows the tray size.

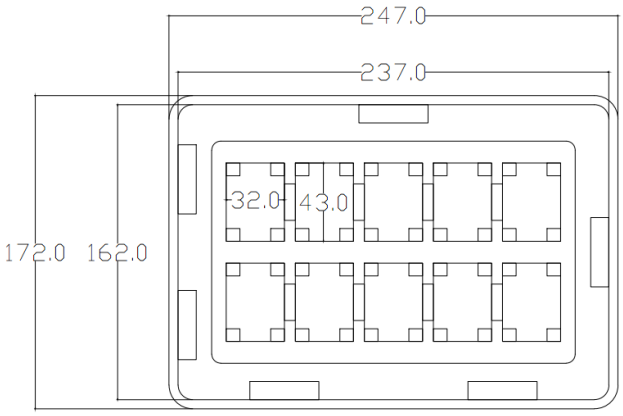


Figure 39: Tray Size (Unit: mm)

Each tray contains 10 modules. The smallest package contains 100 modules. Tray packaging procedures are as below.

1. Use 10 trays to package 100 modules at a time (tray size: 247 mm × 172 mm).
2. Place an empty tray on the top of the 10-tray stack.
3. Fix the stack with masking tape in "#" shape as shown in the following figure.
4. Pack the stack with conductive bag, and then fix the bag with masking tape.
5. Place the list of IMEI No. into a small carton.
6. Seal the carton and then label the seal with sealing sticker (small carton size: 250 mm × 175 mm × 128 mm).

Figure 40: Tray Packaging Procedure

8 Appendix References

Table 47: Related Documents

SN.	Document Name	Description
[1]	Quectel_RM500Q_Series_Reference_Design	RM500Q-GL reference design
[2]	Quectel_RM50xQ-GL_CA&EN-DC_Features	CA&ENDC combinations of RM500Q-GL
[3]	Quectel_PCIe_Card_EVB_User_Guide	PCIe card EVB user guide
[4]	Quectel_RG50xQ&RM5xxQ_Series_AT_Commands_Manual	AT commands manual for RG50xQ series and RM5xxQ series
[5]	Quectel_RM500Q_Series+IPQ8074A_Reference Design	RM500Q+IPQ8074A reference design
[6]	Quectel_RG50xQ&RM5xxQ_Series_GNSS_Application_Note	The GNSS application note for RG50xQ and RM5xxQ series

Table 48: Terms and Abbreviations

Abbreviation	Description
BIOS	Basic Input Output System
bps	Bit Per Second
BW	Bandwidth
CHAP	Challenge-Handshake Authentication Protocol
COEX	Coexistence
CPE	Customer Premise Equipment
CSQ	Cellular Signal Quality
DC-DC	Direct Current to Direct Current
DC-HSDPA	Double Carrier-High-Speed Downlink Packet Access

DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DPR	Dynamic Power Reduction
DRX	Discontinuous Reception (***Chapter 3.1.1***) Diversity Reception (***Chapter 5***)
EIRP	Equivalent Isotropically Radiated Power
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FDD	Frequency Division Duplexing
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	Generic RF Control
GSM	Global System for Mobile Communications
HPUE	High Power User Equipment
HSPA(+)	High Speed Packet Access(+)
HSUPA	High Speed Uplink Packet Access
kbps	Kilo Bits Per Second
LAA	License-Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
MBIM	Mobile Broadband Interface Model
Mbps	Mega Bits Per Second
ME	Mobile Equipment
MHB	Mid-to-High Band
MIMO	Multiple-Input Multiple-Output

MLCC	Multilayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Signification Bit
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QMI	Qualcomm MSM (Mobile Station Modems) Interface
RC	Root Complex
RF	Radio Frequency
RFFE	RF Front-End
R/LHCP	Right/Left Hand Circular Polarization
Rx	Receive
SAR	Specific Absorption Rate
SCS	Subcarrier Spacing
SDR	Software-Defined Radio
SIMO	Single-Input Multiple-Output
SMS	Short Message Service
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UHB	Ultra-High Band
UL	Uplink

URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	Input High Voltage Level
V_{IL}	Input Low Voltage Level
V_{OH}	Output High Voltage Level
V_{OL}	Output Low Voltage Level
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network